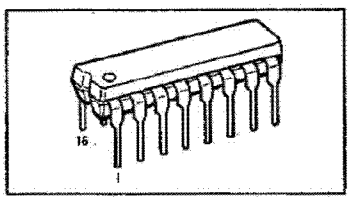
NMB Semiconductor

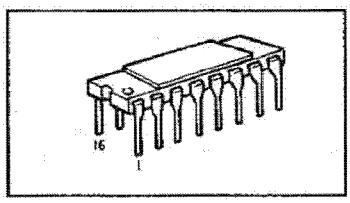
AAA2801
PAGE MODE
CMOS 256K×1 Dynamic RAM

FEATURES

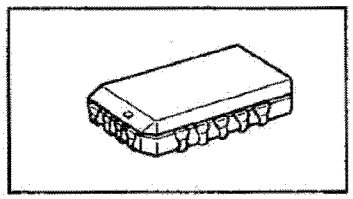
- 262,144 words x 1 bit organization
- Ultra high speed, 60, 70, 80, 100 ns $\overline{RAS}$ access times over full V_{CC} (4.5V to 5.5V) and temperature (0°C to 70°C) ranges
- Eliminates traditional DRAM multiplexed address timing constraints
- Advanced field shield isolated CMOS process optimized for speed
- Inputs and outputs are CMOS and TTL compatible
- Extended $\overline{RAS}$ active time to facilitate multiple accesses within a row
- Low power (CMOS input levels)
  Standby: 12.5 mW
  Active: 275 mW at 100ns access time
- 4.4 ms, 256 cycle refresh
- Single 5V ± 10% supply
- JEDEC standard pinout
- $\overline{CAS}$-before-$\overline{RAS}$ refresh as well as $\overline{RAS}$-Only refresh



PLASTIC PACKAGE



CERAMIC SIDEBRAZED PACKAGE


PALSTIC LEADED CHIP CARRIER

DESCRIPTION

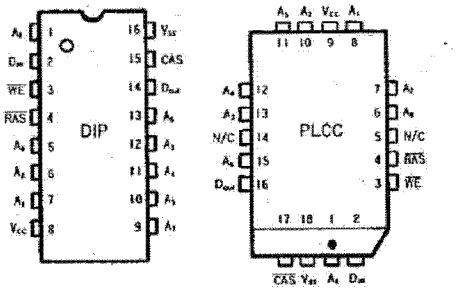
The AAA2801 is a 256K x 1 Dynamic RAM product designed and processed for ultra high performance. The AAA2801 is fabricated with advanced CMOS technology resulting in high speed, low power and extremely wide operating margins.

The AA2801 has a Page mode of operation, it allows random or sequential access of up to 512 bits within a row.

The AAA2801 chip design uses asynchronous column address decoding as well as on-chip transparent row address latch which permits an extremely short row address capture time (4ns; 2ns set-up and 2ns hold). This relieves the system designer of the constraint of timing overhead associated with address multiplexing, and makes it possible to achieve system $\overline{RAS}$ access times as fast as 60 ns which allows interfacing to the next generation of high speed microprocessors.

The AAA2801 is a cost effective VLSI DRAM for applications that demand high density, reliability, high performance and wide operating margins.

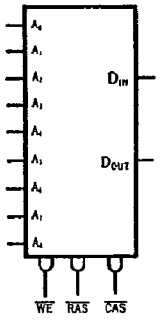
PIN CONFIGURATION



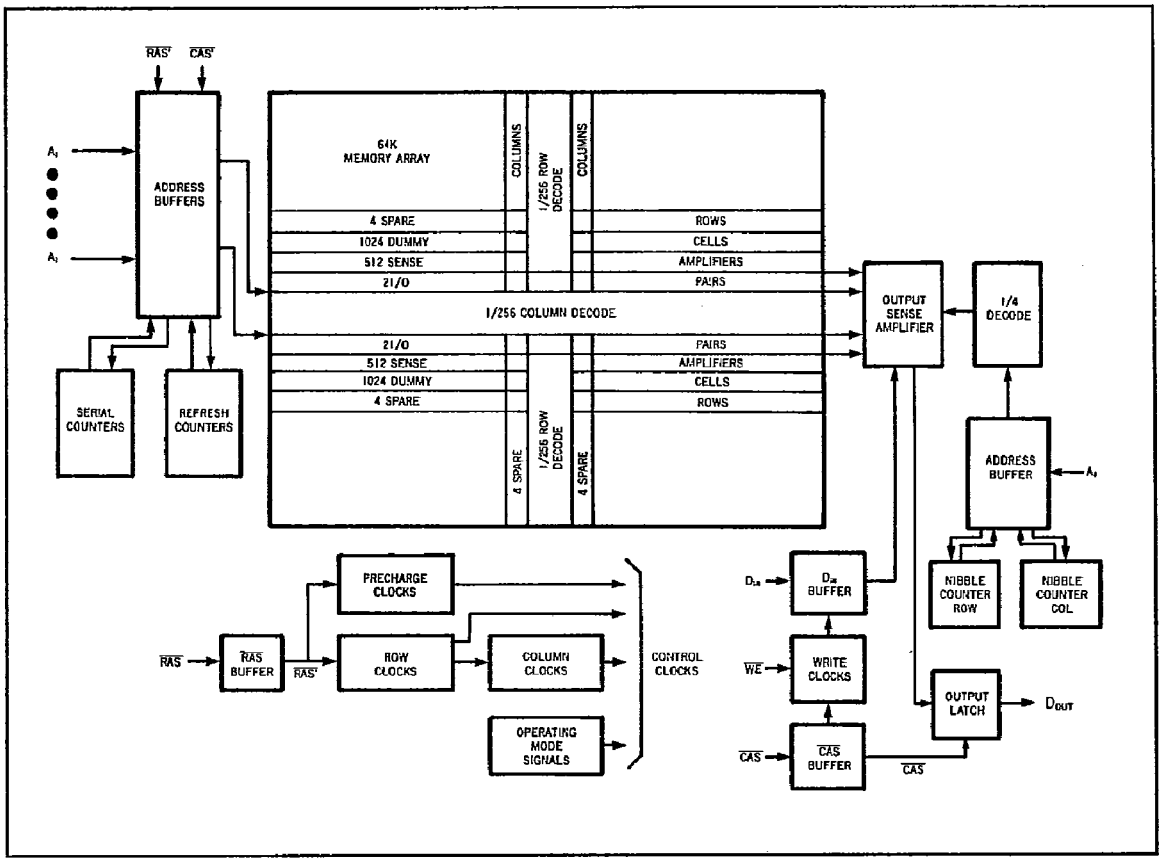
PIN NAMES

A_0-A_8	ADDRESS INPUTS
$\overline{CAS}$	COLUMN ADDRESS STROBE
$\overline{RAS}$	ROW ADDRESS STROBE
D_{in}	DATA IN
D_{out}	DATA OUT
$\overline{WE}$	WRITE ENABLE
V_{CC}	+5V SUPPLY INPUT
V_{SS}	GROUND

LOGIC SYMBOL



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*[a]

RATING	SYMBOL	VALUE	UNIT
Voltage on V_{CC} Relative to V_{SS}	V_{CC} Vin, Vout	−1 to 7	V
Storage Temperature (Ceramic)	Tstg 1	−65 to 150	°C
Storage temperature (Plastic)	Tstg 2	−55 to 125	°C
Power Dissipation	Pd	1.0	W
Data out Current (Short Circuit)	Iout	50	mA

*Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC OPERATING CONDITIONS [a,b]

SYMBOL	PARAMETER	MIN	NOM	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage		0		V	
V_{IH}	Logic "1" Voltage	2.4		6.5	V	
V_{IL}	Logic "0" Voltage	−1.0		0.8	V	
T_A	Ambient Operating Temperature	0		70	°C	Still Air

Note:

a: All voltage values in this data sheet are with respect to V_{SS}.

b: After power-up, a pause of 1 ms followed by eight initialization memory cycles is required to achieve proper device operation.
Any interval greater than 4.4ms with $\overline{RAS}$ inactivity requires eight reinitialization cycles to achieve proper device operation.

DC ELECTRICAL CHARACTERISTICS ($0°C \le T_A \le 70°C$, $V_{CC} = 5.0V \pm 10\%$)

SYMBOL	PARAMETER		MIN	MAX	UNIT	NOTES
I_{CC1}	Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling; $t_{RC} = t_{RCmin}$)	2801-06	—	75	mA	a
		2801-07	—	70	mA	
		2801-08	—	65	mA	
		2801-10	—	55	mA	
I_{CC2}	Standby Current: All Inputs Stable at CMOS Levels, $\overline{RAS} \ge (V_{CC} - 0.4V)$		—	2.5	mA	b
	$\overline{RAS} = \overline{CAS} = V_{IH}$, D_{OUT} = HiZ		—	3.0	mA	
	$\overline{RAS} = V_{IH}$, $\overline{CAS} = V_{IL}$, D_{OUT} = Enable		—	3.0	mA	
	All Inputs Stable at TTL Levels, $\overline{RAS} \ge 2.4V$		—	4.5	mA	
	All Inputs Toggling Between CMOS Levels at 6.25 MHZ, $\overline{RAS} \ge (V_{CC} - 0.4V)$		—	4.0	mA	b
	All Inputs (Except $\overline{RAS}$) Toggling Between TTL Levels at 6.25 MHz		—	5.5	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current ($\overline{RAS}$ Cycling, $\overline{CAS} = V_{IH}$; $t_{RC} = t_{RCmin}$)	2801-06	—	65	mA	c
		2801-07	—	60	mA	
		2801-08	—	55	mA	
		2801-10	—	45	mA	
I_{CC4}	Average Power Supply Current for page mode ($t_{RSC} = t_{WSC}$, both at minimum)	2801-06	—	35	mA	a
		2801-07	—	30	mA	
		2801-08	—	27	mA	
		2801-10	—	25	mA	
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current ($\overline{RAS}$, $\overline{CAS}$ Cycling; $t_{RC} = t_{RCmin}$)	2801-06	—	65	mA	c
		2801-07	—	60	mA	
		2801-08	—	55	mA	
		2801-10	—	45	mA	
I_{LI}	Input Leakage Current (Any Input), $0V \le V_{IN} \le 5.5V$, others = 0V		−10	10	µA	
I_{LO}	Output Leakage, D_{OUT} = HiZ, $0V \le V_{OUT} \le 5.5V$		−10	10	µA	
V_{OH}	Output High Voltage, $I_O = -5.0mA$		2.4		V	
V_{OL}	Output Low Voltage, $I_O = 5.0mA$			0.4	V	

Notes:

a. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with output open.

b. CMOS levels are defined as V_{IH} (min) ≥ (V_{CC} - 0.4V) and V_{IL} (max) ≤ 0.4V.
TTL levels are defined as V_{IH} (min) ≥ 2.4V and V_{IL} (max) ≤ 0.8V.

c. I_{CC} is dependent on cycle rates.

AC TEST CONDITIONS

Input Pulse Levels	0 to 3V
Input Rise and Fall Times	3ns between 0.8 and 2.4V
Input Timing Reference Levels	0.8 and 2.4V
Output Timing Reference Levels	0.8 and 2.4V
Output Load	Equivalent to 2 TTL Loads and 50pF

CAPACITANCE

SYMBOL	PARAMETER	MAX	UNITS	COND
C_{IN}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	6	pF	a
C_{IN}	Input Cap. Addresses	5	pF	a
C_{OUT}	Output Cap.	7	pF	a,b

Note:

a: Capacitance measured with Boonton Meter

b: $\overline{CAS} = V_{IH}$ to disable D_{OUT}

AC OPERATING CONDITIONS ($0°C \le T_A \le 70°C$, $V_{CC} = 5V \pm 10\%$)

NO.	PARAMETER	SYMBOL		2800-06		2800-07		2800-08		2800-10		UNIT	NOTES
		JEDEC	STD	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
1	Column Address Set-Up	t_{AVCL2}	t_{ASC}	0		0		0		0		ns	
2	Row Address Set-Up	t_{AVRL2}	t_{ASR}	2		2		2		2		ns	
3	Column Address to $\overline{WE}$ Delay	t_{AVWL2}	t_{AWD}	32		35		40		45		ns	c.g
4	Output Turn-Off Delay	t_{CH2QZ}	t_{OFF}		17		18		19		21	ns	a
5	$\overline{CAS}$ to $\overline{RAS}$ Precharge	t_{CH2RL2}	t_{CRP}	3		3		3		3		ns	
6	Read Command Hold (Reference $\overline{CAS}$)	t_{CH2WX}	t_{RCH}	0		0		0		0		ns	b
7	Column Address Hold	t_{CL1AX}	t_{CAH}	6		7		8		9		ns	
8	$\overline{CAS}$ Pulse Width (Read)	t_{CL1CH1}	t_{CAS}	11		12		14		16		ns	
9	$\overline{CAS}$ Pulse Width (Write)	t_{CL1CH1}	t_{CAS}	5		5		5		5		ns	
10	Data-In Hold Time from $\overline{CAS}$	t_{CL1DX}	t_{DH}	6		7		8		9		ns	c
11	$\overline{CAS}$ Access	t_{CL1QV}	t_{CAC}		11		12		13		16	ns	
12	$\overline{RAS}$ Hold Time	t_{CL1RH1}	t_{RSH}	15		18		20		25		ns	
13	$\overline{CAS}$ Setup ($\overline{CAS}$ Before $\overline{RAS}$ Refresh)	t_{CL1RL2}	t_{CSR}	2		2		2		2		ns	
14	$\overline{CAS}$ Write Hold (Reference $\overline{CAS}$)	t_{CL1WH1}	t_{WCH}	5		5		5		5		ns	
15	$\overline{CAS}$ to $\overline{WE}$ Delay (Read-Modify-Write)	t_{CL1WL2}	t_{CWD}	11		12		13		16		ns	d
16	Data Set-Up (Early Write)	t_{DVCL2}	t_{DS}	0		0		0		0		ns	c
17	Data Set-Up (Late Write)	t_{DVWL2}	t_{DS}	0		0		0		0		ns	c
18	$\overline{RAS}$ to Column Address Delay Time	t_{RL1AV}	t_{RAD}	4	28	4	35	4	40	4	55	ns	h
19	$\overline{RAS}$ Precharge	t_{RH2RL2}	t_{RP}	55		65		75		80		ns	
20	Read Command Hold (Reference $\overline{RAS}$)	t_{RH2WX}	t_{RRH}	0		0		0		0		ns	b
21	Column Address Hold (Reference $\overline{RAS}$)	t_{RL1AX}	t_{AR}	40		43		45		50		ns	
22	Row Address Hold	t_{RL1AX}	t_{RAH}	2		2		2		2		ns	
23	$\overline{CAS}$ Hold ($\overline{CAS}$-Before-$\overline{RAS}$)	t_{RL1CH1}	t_{CHR}	2		2		2		2		ns	
24	$\overline{CAS}$ Hold Time (Early Write)	t_{RL1CH1}	t_{CSH}	40		43		45		50		ns	
25	$\overline{RAS}$ to $\overline{CAS}$ Delay	t_{RL1CL1}	t_{RCD}	6	45	6	55	6	65	6	80	ns	i
26	Data in Hold (Reference $\overline{RAS}$)	t_{RL1DX}	t_{DHR}	40		43		45		50		ns	
27	$\overline{RAS}$ Access	t_{RL1QV}	t_{RAC}		60		70		80		100	ns	
28	$\overline{RAS}$ Pulse Width	t_{RL1RH1}	t_{RAS}	60	10^5	65	10^5	70	10^5	90	10^5	ns	
29	Write Command Hold (Reference $\overline{RAS}$)	t_{RL1WH1}	t_{WCR}	40		43		45		50		ns	
30	$\overline{RAS}$ to $\overline{WE}$ Delay (Read-Modify-Write)	t_{RL1WL2}	t_{RWD}	60		70		80		100		ns	d
31	Random Read-Write Cycle	t_{RL2RL2}	t_{RC}	121		136		151		176		ns	
32	Read Command Set-Up	t_{WH2CL2}	t_{RCS}	0		0		0		0		ns	d
33	Write Command to $\overline{CAS}$ Lead	t_{WL1CH1}	t_{CWL}	5		5		5		5		ns	
34	Early Write $\overline{WE}$ Set-Up	t_{WL1CL2}	t_{WCS}	0		0		0		0		ns	d
35	Data-In Hold (Late Write)	t_{WL1DX}	t_{DH}	5		6		7		8		ns	c
36	Write Command to $\overline{RAS}$ Lead	t_{WL1RH1}	t_{RWL}	13		15		17		22		ns	
37	Write Pulse	t_{WL1WH1}	t_{WP}	5		5		5		5		ns	
38	Refresh Period	t_{REF}	t_{REF}		4.4		4.4		4.4		4.4	ms	
39	Transition Time (Rise and Fall)	t_T	t_T	2	50	2	50	2	50	2	50	ns	e.f
40	Output Hold from $\overline{WE}$	t_{WL1QX}	t_{OHW}	5		5		5		5		ns	
41	Column Address Access	t_{AVQV}	t_{AA}		32		35		40		45	ns	d
42	Page Read/Write Cycle	t_{CL2CL2}	t_{PC}	37		41		46		51		ns	
43	Acorss from $\overline{CAS}$ Precharge	t_{CH2QV}	t_{CAP}		34		38		43		48	ns	
44	$\overline{CAS}$ Precharge(Page)	t_{CH2CL2}	t_{CP}	5		5		5		5		ns	

AC OPERATING CONDITIONS ($0°C \le T_A \le 70°C$, $V_{CC} = 5V \pm 10\%$)

NO.	PARAMETER	SYMBOL		2800-06		2800-07		2800-08		2800-10		UNIT	NOTES
		JEDEC	STD	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
45	RMW Cycle Time	t_{RL2RL2}	t_{RWC}	134		151		168		198		ns	
46	Output Data Hold Time from $\overline{CAS}$	t_{CH1QX}	t_{OH}	2		2		2		2		ns	
47	$\overline{CAS}$ Hold time (Read)	t_{RL1CH1}	t_{CSH}	60		70		80		100		ns	
48	$\overline{RAS}$ Precharge - $\overline{CAS}$ Hold Time(CBR)	t_{RH2CL2}	t_{RPC}	0		0		0		0		ns	

Notes:

a. t_{OFF} is defined as the time at which the output achieves the open circuit condition.

b. Either t_{CH2WX} or t_{RH2WX} must be satisfied for a Read cycle.

c. Address and data set-up and hold times referenced to $\overline{CAS}$ (t_{DVCL2}, t_{CL1DX}) are restrictive parameters for Early-Write operations only. Address and data set-up times referenced to $\overline{WE}$ (t_{AVWL2}, t_{DWCL2}, and t_{WL1DX}) are restrictive parameters for Read-Modify-Write cycle operations.

d. t_{WH2CL2}, t_{CL1WL2}, and t_{RL1WL2} are restrictive operating parameters in Read-Write and Read-Modify-Write cycles only.
If $t_{WL1CL2} \ge t_{WL1CL2}$ (min) the cycle is an Early-Write cycle and data will remain open circuit unless $\overline{WE}$ goes high while $\overline{CAS}$ and $\overline{RAS}$ are both low.
If $t_{WH2CL2} \ge t_{WH2CL2}$ (min), $t_{RL1WL2} \ge t_{RL1WL2}$ (min), and $t_{AVQV} \ge t_{AVQV}$ (min) the cycle is a Read-Write and the data ouput will contain data read from the selected cell.
If neither of the above conditions is met, the conditions of the data out is indeterminate at access time and remains so until either $\overline{CAS}$ or $\overline{WE}$ returns to V_{IH}.

e. The transition time specification applies for all input signals.
In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
Transition time is measured between V_{IL} (max) and V_{IH} (min).

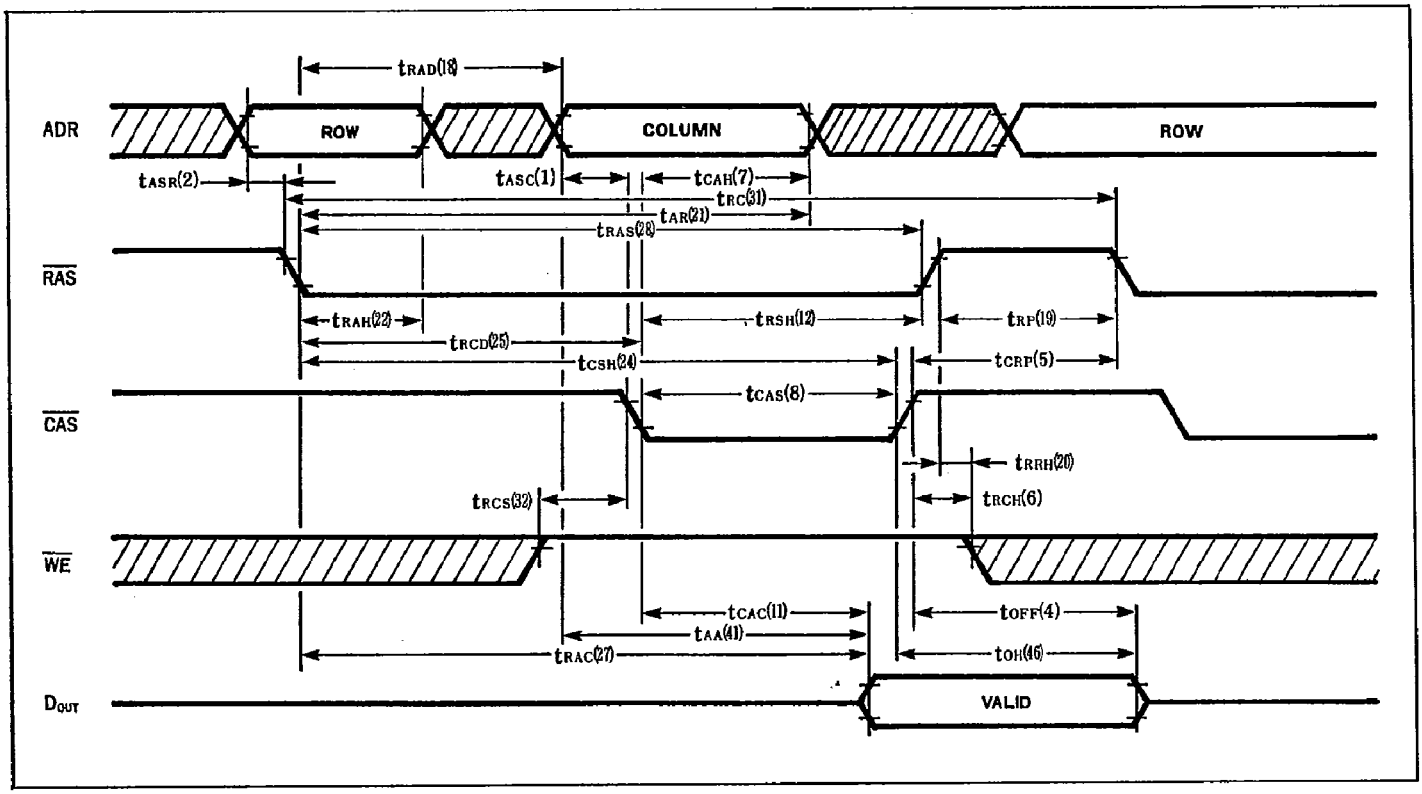
f. 3ns rise and fall times (t_T) are used for cycle time specifications.

g. t_{AVWL2} is restrictive parameter for Read-Modify write cycles when read access prior to write is required.

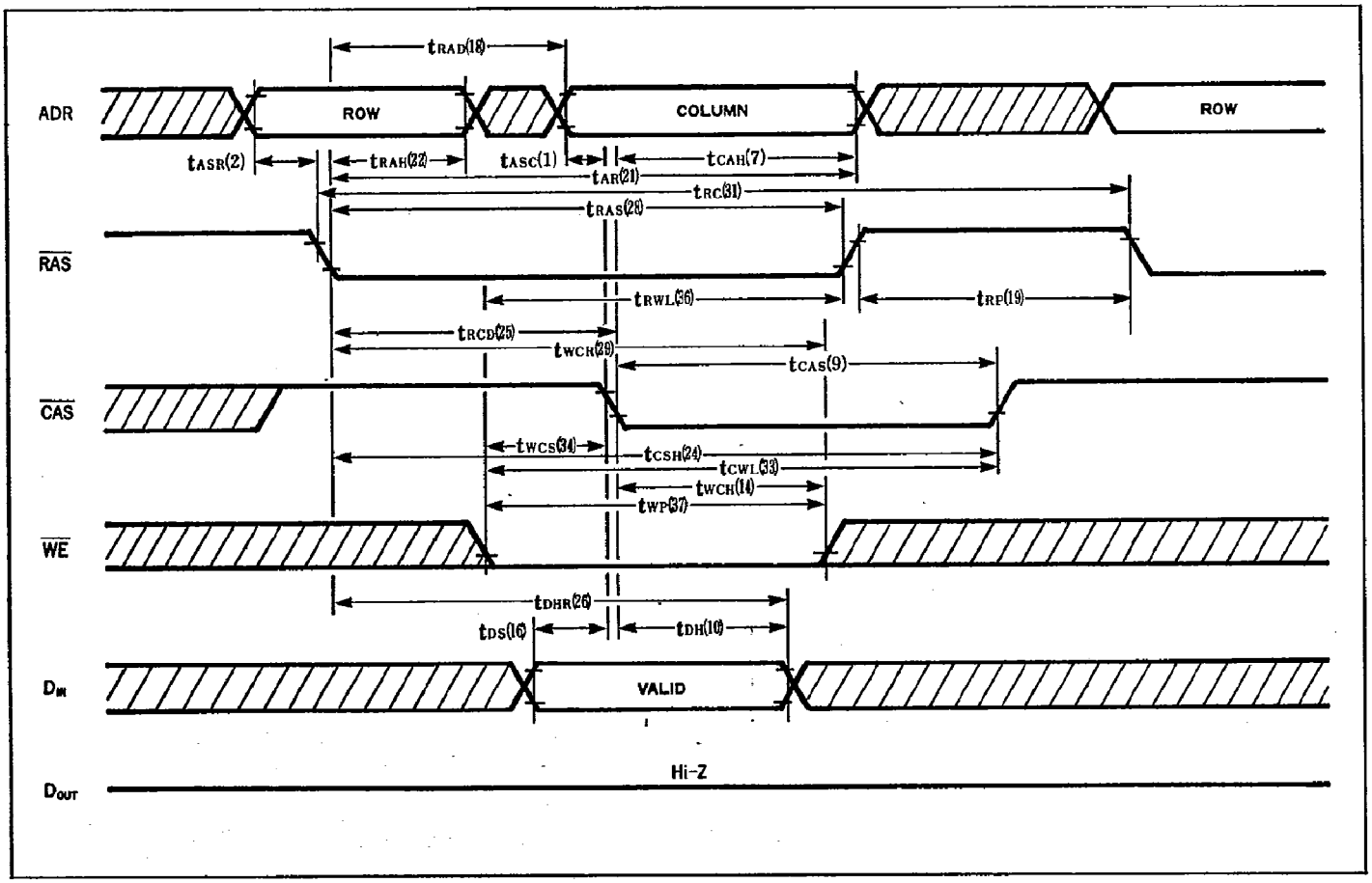
h. Operation within the t_{RL1AV} (max) limit insures that t_{RL1QV} (max) can be met. t_{RL1AV} (max) is specified as a reference point only. If t_{RL1AV} is greater than the specified t_{RL1AV} (max) limit, then the access time is controlled by t_{AVQV} and t_{CL1QV}.

i. t_{RL1CL1} (max) is specified for reference only. Operation within t_{RL1CL1} (max) and t_{RL1AV} (max) limit insure that t_{RL1QV} (max), t_{AVQV} (max) can be met. If t_{RL1CL1} is greater than the specified t_{RL1CL1} (max) then the access time is controlled by t_{AVQV} and t_{CL1QV}.

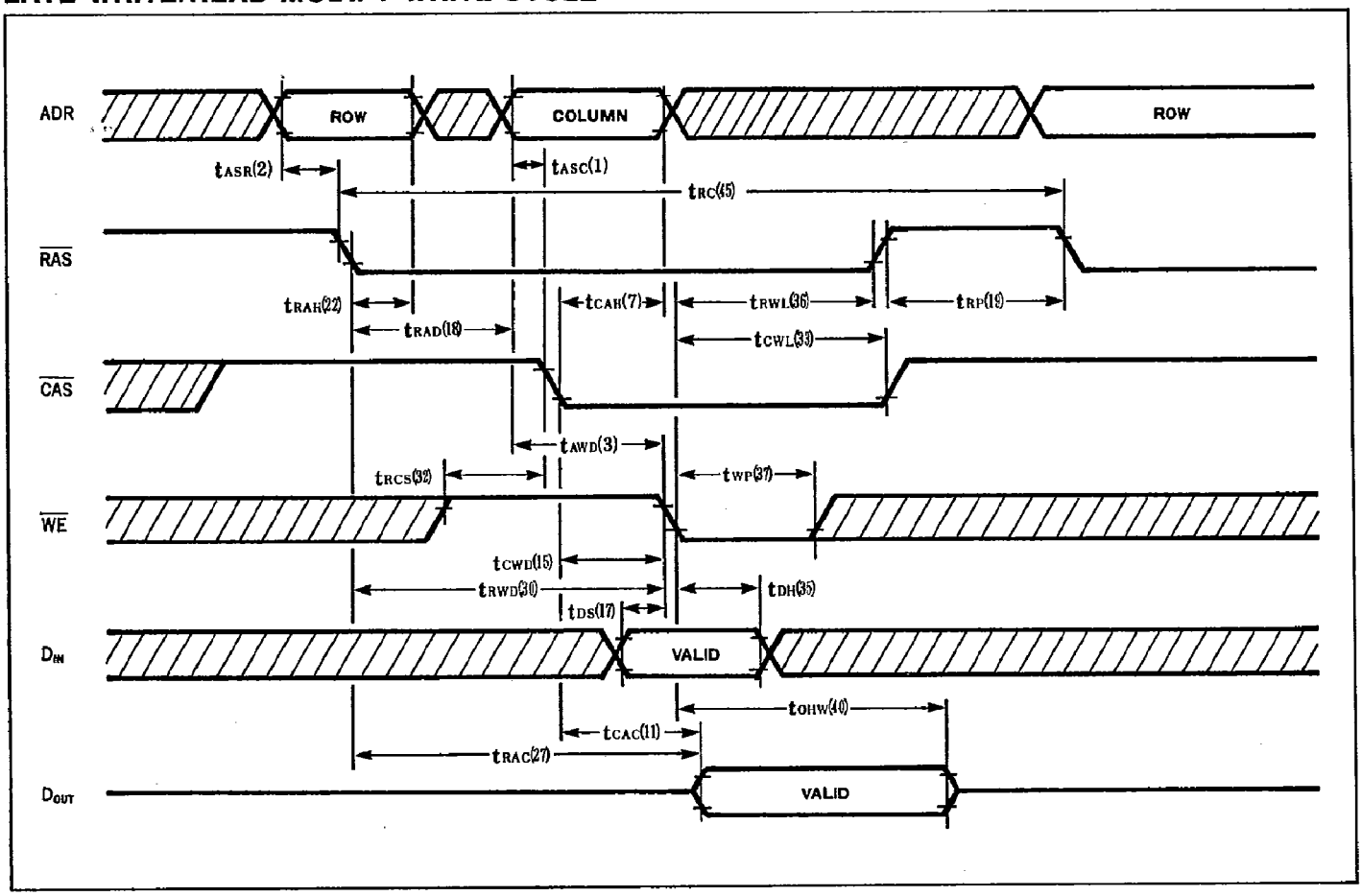
READ CYCLE



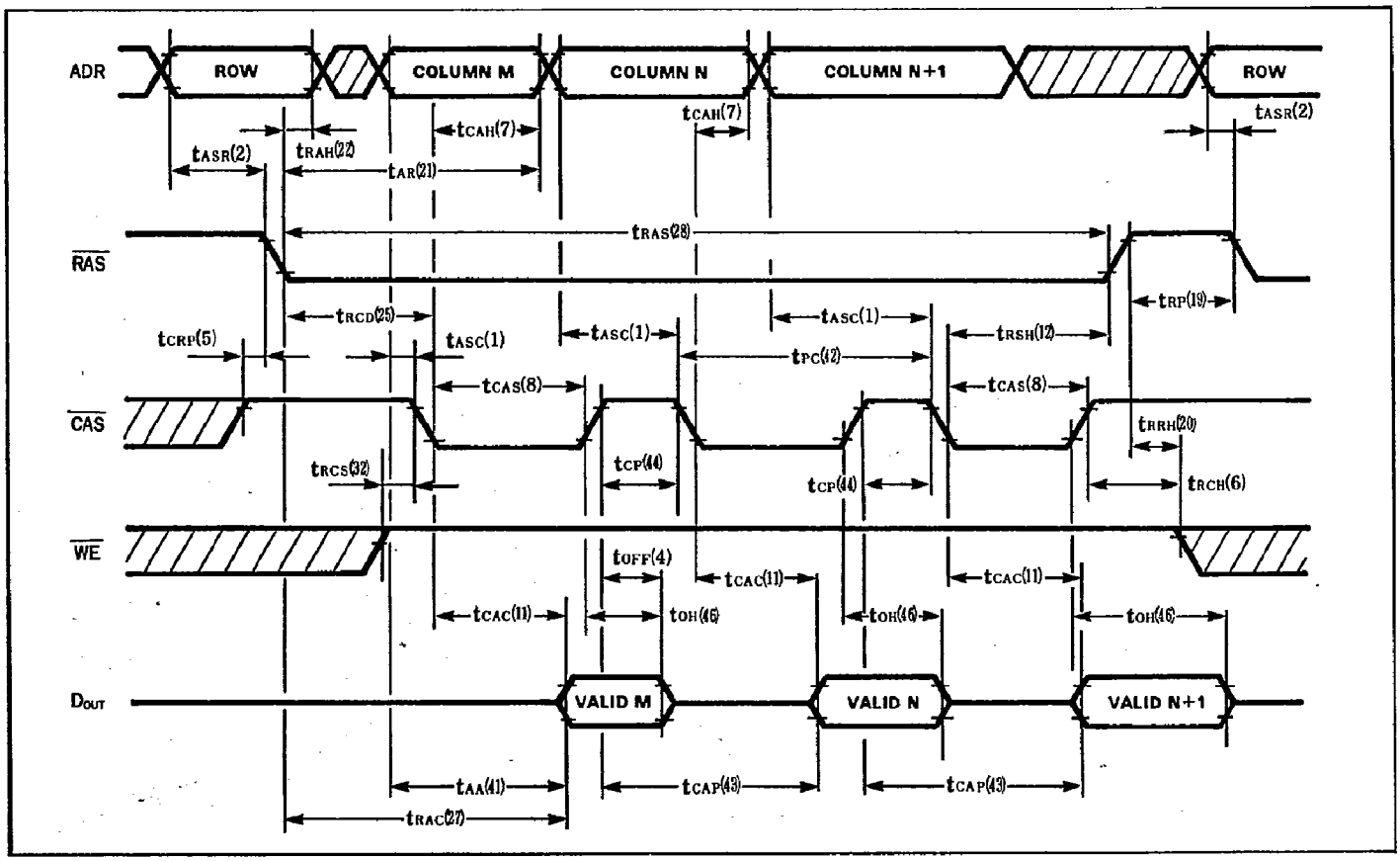
EARLY-WRITE CYCLE



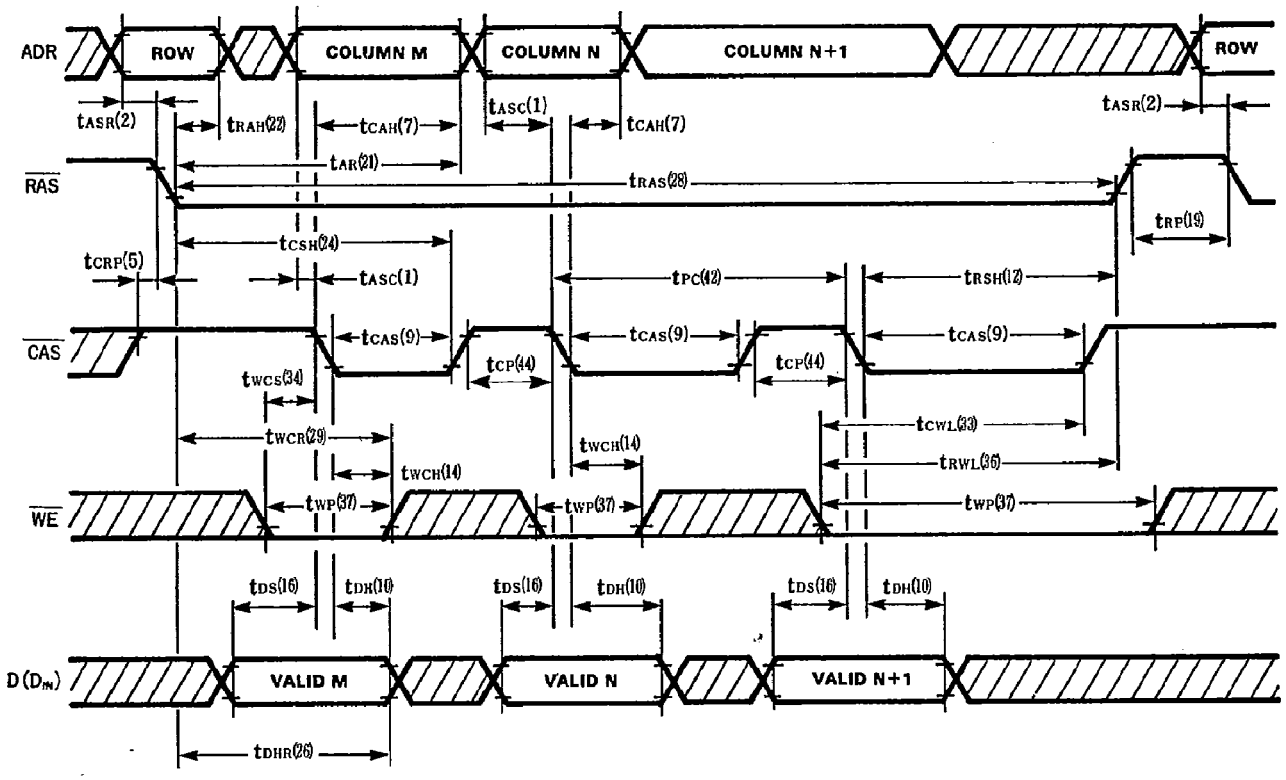
LATE-WRITE/READ-MODIFY-WRITE CYCLE



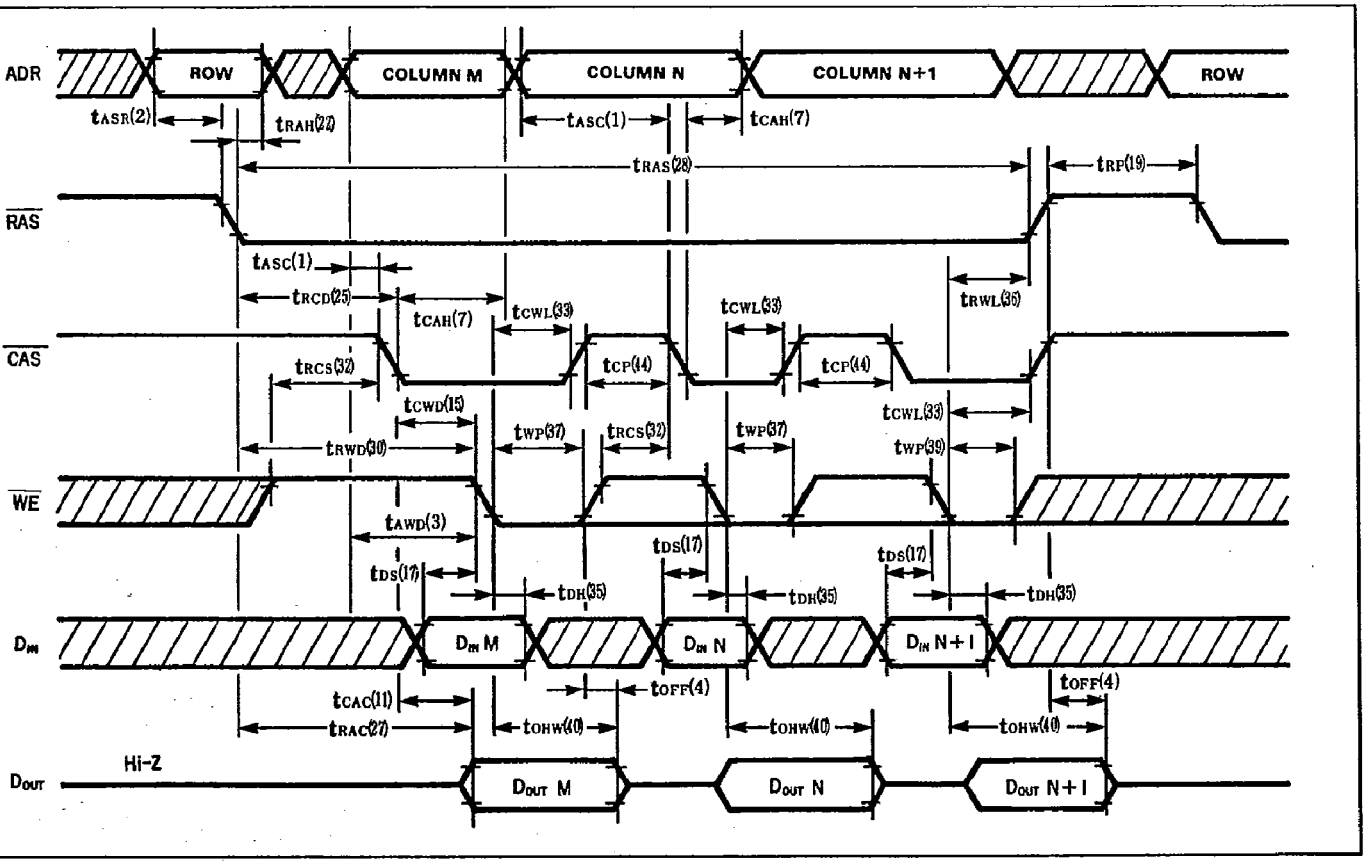
PAGE MODE READ CYCLE



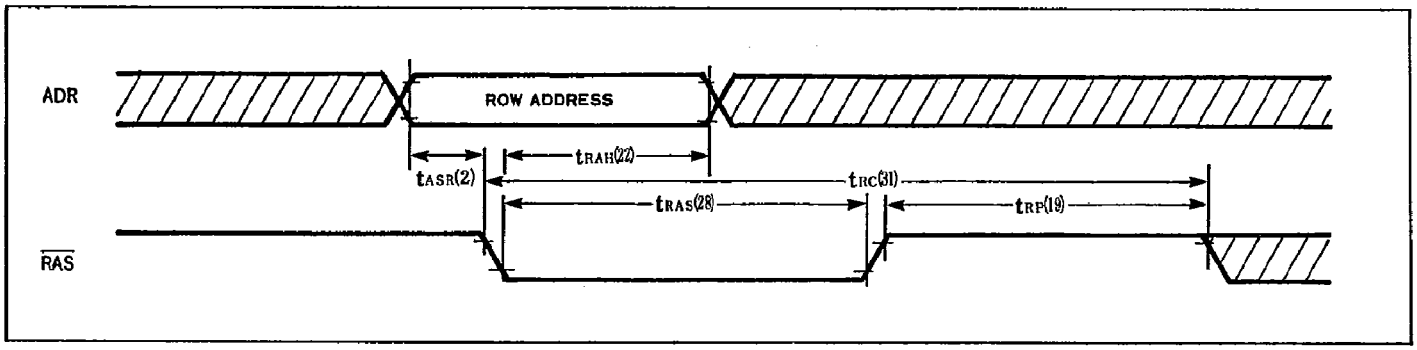
PAGE MODE EARLY-WRITE CYCLE



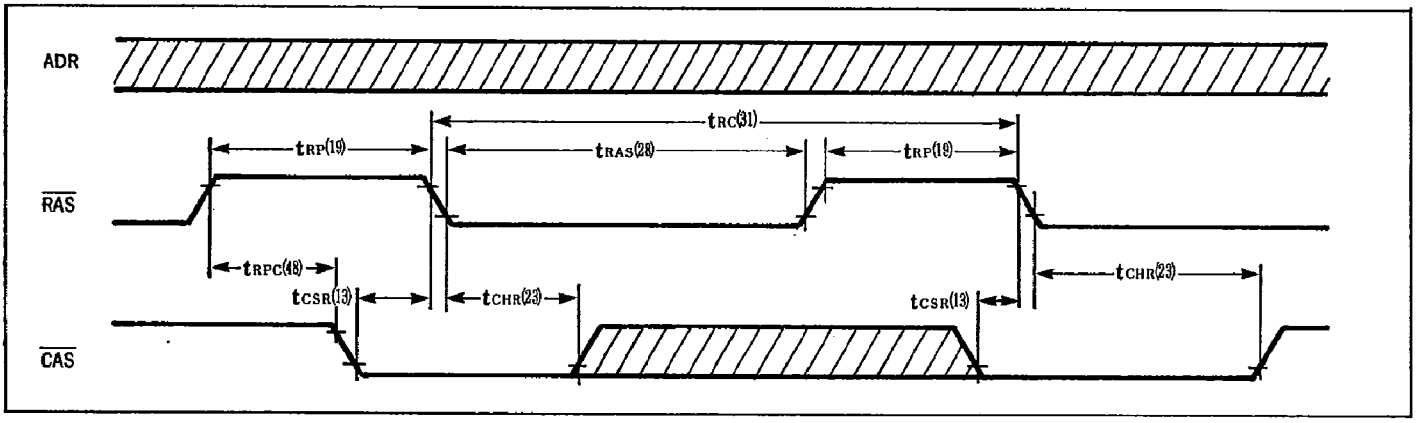
PAGE MODE LATE-WRITE / READ-MODIFY-WRITE CYCLE



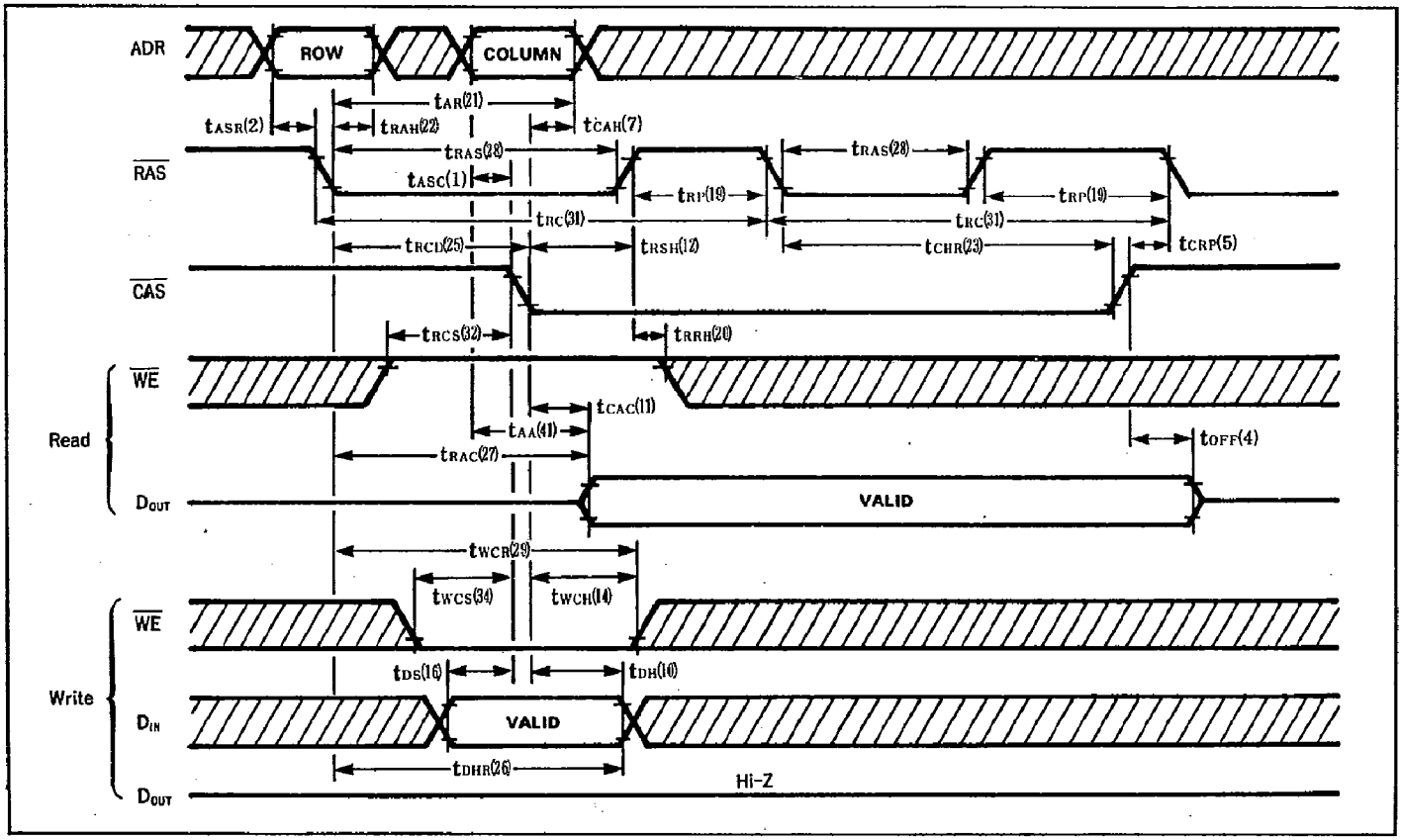
$\overline{\text{RAS}}$-ONLY REFRESH [$\overline{\text{CAS}} \geq V_{IH}$ (MIN)]



$\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH



HIDDEN REFRESH



TIMING INFORMATION

All cycles of the AAA2801 are initiated by a high-to-low transition of $\overline{RAS}$. For Read, Write, Read-Modify-Write, or $\overline{RAS}$-Only refresh cycles, the high-to-low transition of $\overline{RAS}$ causes the state of the 9 external address lines (A_0 through A_8) to be latched. Eight of the nine address bits are decoded to select one of 256 rows. The ninth row address bit (A_8) is saved and becomes part of the ten bit column address which selects one of the 1024 column locations. The AAA2801 uses transparent latches to capture the row addresses which permits an extremely short capture time for the row addresses with only a 2ns set-up and 2ns hold required. After the short row address capture time has been satisfied, the 9 external address lines can be changed to the column address. Column address decoding on the AAA2801 is static (asynchronous or ripple through; Static Column Decoded) when ever $\overline{CAS}$ is high but the column addresses are latched when $\overline{CAS}$ is low. This provides the advantages of statically decoded colunmn accessing while maintaining compatibility with conventional DRAMs. After the high-to-low transition of $\overline{RAS}$, the state of $\overline{CAS}$ and $\overline{WE}$ determine whether the cycle is a Read, Write, Read-Modify-Write, or a $\overline{RAS}$-Only refresh cycle. The cycle is terminated by bringing $\overline{RAS}$ high. A new cycle may be initiated after $\overline{RAS}$ has been high for the specified precharge interval [t_{RH2RL2}(min)]. $\overline{RAS}$ and $\overline{CAS}$ must be properly overlapped and once brought low they must remain low for their specified pulse widths.

Read Cycle

A read cycle is performed on one or more memory locations if $\overline{WE}$ is high while both $\overline{RAS}$ and $\overline{CAS}$ are low. During a read cycle, at access time the output will reflect the contents of the cell addressed by the 9 latched row and column addresses. The read access time is determined by t_{RL1QV}, t_{AVQV}, or t_{CL1QV}, whichever is greatest. When data is accessed, the data output is entirely under the control of $\overline{CAS}$; accessed data will remain valid as long as $\overline{CAS}$ remains active even if a $\overline{RAS}$ sequence occurs while $\overline{CAS}$ is held low.

Write Cycles

A write cycle is initiated when $\overline{WE}$, $\overline{CAS}$ and $\overline{RAS}$ are low. The AAA2801 will perform three types of write cycles: Early-Write, Late-Write and Read-Modify-Write. During a $\overline{RAS}$ active cycle, if $\overline{WE}$ goes low prior to $\overline{CAS}$ going low, an Early-Write cycle is executed. Early-Write cycles are initiated by the falling edge of $\overline{CAS}$ with set-up and hold times for both data-in and column addresses referenced to the falling edge of $\overline{CAS}$. With Early-Write cycles, the data-out will remain open (high impedance state). If $\overline{CAS}$ goes low prior to $\overline{WE}$ going low, a Late-Write cycle is executed. Late-Write cycles are initiated by the falling edge of $\overline{WE}$ with set-up and hold times for both data-in and column addresses referenced to the falling edge of $\overline{WE}$. If $\overline{WE}$ is asserted after a valid read access occurs, the operation is called a Read-Modify-Write cucle. During a Read-Modify-Write cycle, the data-out will reflect the contents of the addressed cell before it was written until the output is turned off (high impedance state) by bringing $\overline{CAS}$ high. The choice of write cycle timing is usually very system dependent and the different modes are made available to accomodate these differences. In general, the Early-Write timing is most appropriate for systems that have a bidirectional data bus. Because Q (data-out) remains inactive during Early-Write cycle, the D (data-in) and the Q (data-out) pins may be tied together without bus contention.

Page Mode Cycles

Page mode operation permits access of up to 512 locations within a single $\overline{RAS}$ active cycle. The multiple locations in the same page can be randomly accessed by simple changing the column address inputs and cycling $\overline{CAS}$. Within a page mode cycle, any combination of Read, Write, Early-Write or Late-Write ,or Read-Modify-Write cycles can be executed. Unlike traditional address multiplexed dynamic RAMs, the AAA2801 transparently latches the column addresses (column addresses are ripple-through decoded whenever $\overline{CAS}$ is high and latched when $\overline{CAS}$ is low) which permits column decoding to occur independently of the assertion of $\overline{CAS}$. Additionally, the falling edge of $\overline{CAS}$ acts as a high speed output enable for read cycles and performs a gating function during write cycles. Transparent column address latching allows high speed page mode accesses to be performed by simply changing the column address inputs whenever a new bit in the current page (defined by the 9 bit address field latched by the falling edge of $\overline{RAS}$) is to accessed and toggling $\overline{CAS}$ high and then low. When $\overline{CAS}$ goes high the data-out buffers are turned off (high impedance) and when $\overline{CAS}$ is active the data-out drivers are turned on. Access during the page mode operation is determined by t_{RL1QV}, t_{AVQV}, and t_{CL1QV}, whichever is greatest.

Refresh Cycles

Dynamic RAMS retain data by storing charge on a capacitor. Since the charge will leak away over a period of time, it is necessary to access the data in the cell (capacitor) periodically in order to fully restore the strored charge while if is still at a sufficiently high level to be properly detected. For the AAA2801. any $\overline{RAS}$ sequence will fully refresh all storage cells within the single row addressed. To ensure that all cells remain sufficiently refreshed, all 256 rows (all binary combinations of address bits A_0 through A_7) must be refreshed every 4.4ms.

The addressing of the rows for refresh may be sourced either externally or internally. If the refresh row addresses are to be provided from an external source, $\overline{CAS}$ must be high when $\overline{RAS}$ goes low. If $\overline{CAS}$ is high when $\overline{RAS}$ goes low, any type of cycle (Read, Write, Read-Modify-Write, or $\overline{RAS}$-Only) will cause the externally addressed row to be refreshed.

If $\overline{CAS}$ is low when $\overline{RAS}$ falls, the AAA2801 will use an intermal 8-bit counter as the source of the row addresses and will ignore $\overline{WE}$ and the external address inputs. $\overline{CAS}$-Before-$\overline{RAS}$ refresh mode is a refresh-only mode. Also, $\overline{CAS}$-Before-$\overline{RAS}$ refresh does not cause device selection and the state of the data-out will remain unchanged as long as $\overline{CAS}$ remains low.

APPLICATIONS

To ensure proper operation of the AAA2801 in a system environment it is recommended that the following guidelines be followed.

Power Distribution

Transient currents are required by dynamic RAMs. These transient current spikes can cause significant power supply and ground noise unless adequate power distribution and decoupling is used. The recommended power distribution scheme combines proper trace layout and placement of decoupling capacitors. The impedance in the decoupling path from the power pin (8) through the decoupling capacitor, to the ground pin (16) should be kept to a minimum. The impedance of this path is determined by the series impedance of the power line and the decoupling capacitor.

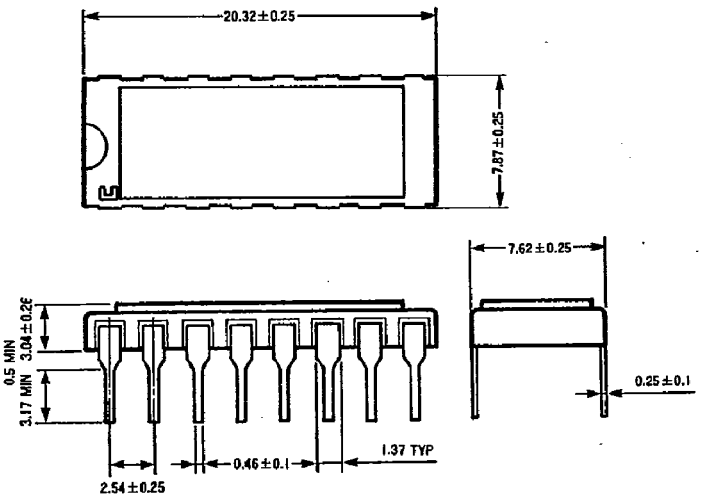
To reduce the power line impedance, it is recommended that the power trace and ground trace be gridded or provided by separate power planes. To prevent loss of signal margins due to differential ground noise, the ground grid of the memory array should be extended to the TTL drivers in the peripheral circuitry. A high-frequency decoupling capacitor with a value of 0.1µF, should be placed between the rows of memory devices in the array. A larger tantalum capacitor with a value between 22µF and 47µF should be placed near the memory board edge connection where the power traces meet the backplane power distribution system. These large capacitors provide bulk energy storage to prevent voltage drop due to the main supply being located off the memory board and at the end of a long inductive path.

Termination

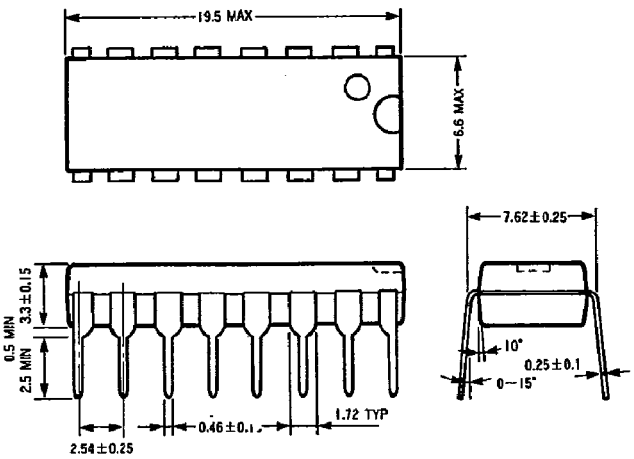
Trace lines on a memory board in the array look to TTL driver signals like low impedance, unterminated transmission lines. In order to reduce or eliminate the reflections of the TTL signals propagating down the lines, especially low-going TTL signals, line termination is recommended. The termination may be either parallel or series but the series termination technique has the advantages of drawing no DC current and using a minimum of components. The recommended technique is to use series termination. A series resistor in the signal line at the output of the TTL driver to match the source impedance of the TTL driver to the signal line will dampen the reflections on the line. The line should be kept short with the driver/termination combination close to the memory array. Some experimentation will have to be done to find the proper value to use for the series termination to minimize reflections, but generally a series resistor in the 10Ω to 30Ω range will be required.

Proper power distribution techniques, including adequate use of decoupling capacitors, along with proper termination of TTL driver outputs, are among the most important, yet basic guidelines to be followed. These guidelines are intended to maintain the operation margins of all devices on the memory board by providing a quiet environment relatively free of noise spikes and signal reflections.

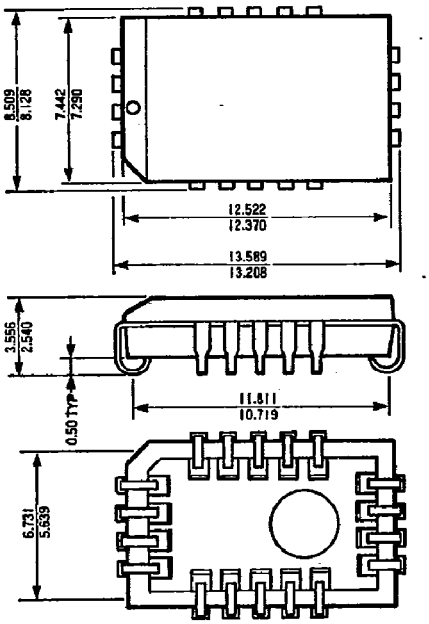
16 PIN SIDEBRAZED (UNIT: mm)



16 PIN PLASTIC DIP (UNIT: mm)



18 PIN PLCC (UNIT: $\frac{\text{MAX}}{\text{MIN}}$ mm)



ORDERING INFORMATION

AAA 280 X X X X

SPEED	06: 60 NANO SECONDS 07: 70 08: 80 10: 100
PACKAGE	P: PLASTIC DIP C: SIDEBRAZE J: PLCC
OPERATION MODE	0: STATIC COLUMN DECODE 1: PAGE 2: NIBBLE 3: BYTE 4: EXTENDED SERIAL

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