

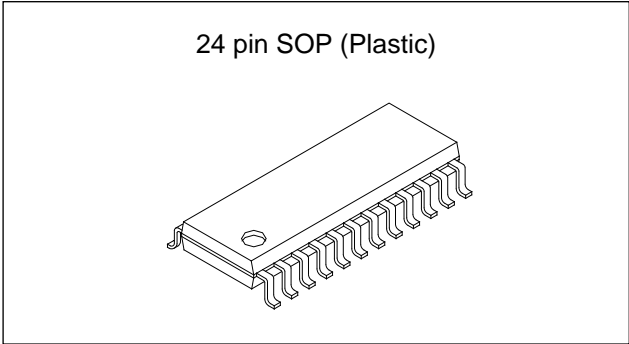
# CXL1503M/1505M

## CMOS-CCD Signal Processor

**Description**

CXL1503M/1505M are CMOS-CCD signal processors developed for CCD camera complementary color filter array processing system.

- CXL1503M 1H × 4 301.5 bit CCD delay line
- CXL1505M 1H × 4 453.5 bit CCD delay line



**Features**

- Single power supply 5V
- Low power consumption
  - CXL1503M 100mW (Typ.)
  - CXL1505M 150mW (Typ.)
- Built-in peripheral circuits
- Built-in CDS (Correlated Double Sampling) circuit

**Function**

- Clock driver
- Autobias circuit (center and black)
- Pedestal clamp circuit
- CDS circuit

**Structure**

CMOS-CCD

**Absolute Maximum Ratings** (Ta = 25°C)

- Supply voltage  $V_{DD}$  6 V
- Operating temperature  $T_{opr}$  -10 to +60 °C
- Storage temperature  $T_{stg}$  -55 to +150 °C
- Allowable power dissipation  $P_D$  500 mW

**Recommended Operating Conditions** (Ta = 25°C)

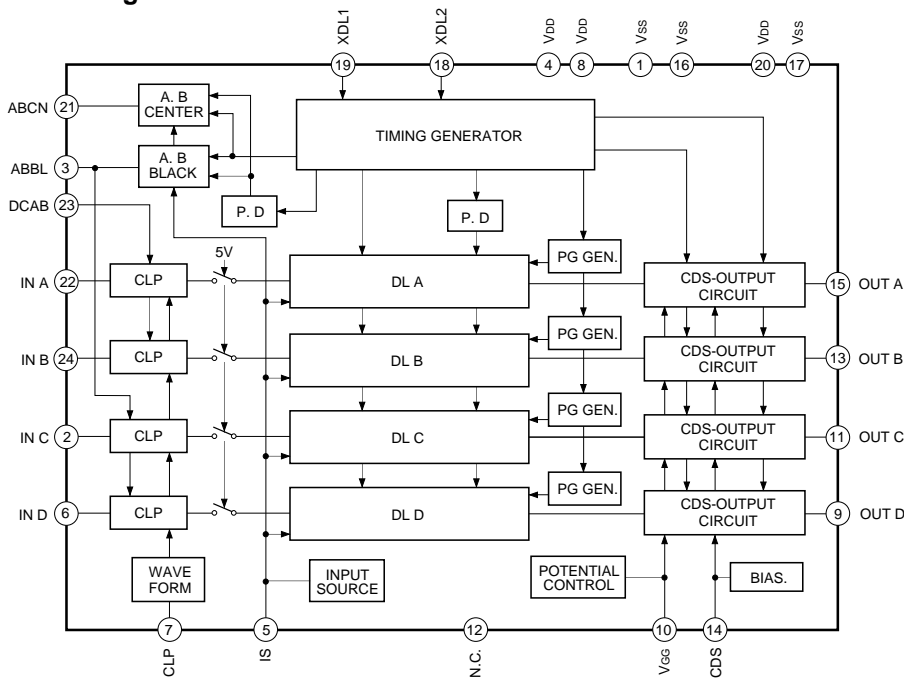
- Supply voltage  $V_{DD}$  5 ± 5% V

**Recommended Clock Conditions** (Ta = 25°C)

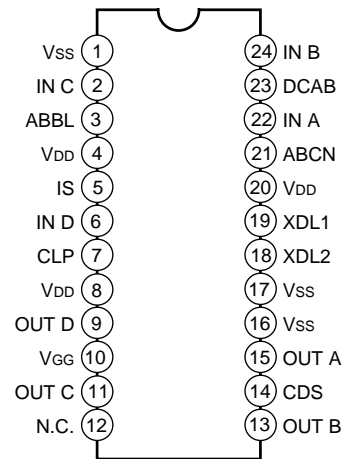
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Clock voltage Low	$V_L$	0		1.0	V	
Clock voltage High	$V_H$	$V_{DD} - 1.0$		$V_{DD}$	V	
Clock frequency	CXL1503M	$f_{CL}$	4.77		MHz	NTSC: 910f <sub>H</sub> /3 CCIR: 908f <sub>H</sub> /3
	CXL1505M	$f_{CL}$	7.16		MHz	NTSC: 455f <sub>H</sub> CCIR: 454f <sub>H</sub>

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Block Diagram



Pin Configuration (Top View)



Pin Description

No.	Symbol	I/O	Description	Impedance ( $\Omega$ )
1, 16, 17	VSS	—	GND	
2	IN C	I	Signal input C channel	> 100k (at no clamp)
3	ABBL	O	Autobias DC output for Y signal	2k to 20k
4, 8, 20	VDD	—	5V power supply	
5	IS	O	Input source DC output	5k
6	IN D	I	Signal input D channel	> 100k (at no clamp)
7	CLP	I	Clamp pulse input	> 100k
9	OUT D	O	Signal output D channel	50 to 500
10	VGG	O	Gate bias DC output	2k to 10k
11	OUT C	O	Signal output C channel	50 to 500
12	N.C.	—	—	
13	OUT B	O	Signal output B channel	50 to 500
14	CDS	O	DC output for CDS	500 to 5k
15	OUT A	O	Signal output A channel	50 to 500
18	XDL2	I	Clock pulse input 2	> 100k
19	XDL1	I	Clock pulse input 1	> 100k
21	ABCN	O	Autobias DC output for C signal	2k to 20k
22	IN A	I	Signal input A channel	> 100k (at no clamp)
23	DCAB	I	DC bias input for A and B channel	> 100k
24	IN B	I	Signal input B channel	> 100k (at no clamp)

Electrical Characteristics

(Ta = 25°C, VDD = 5.0V, VSS = 0V)  
 fCL = 4.77MHz (CXL1503M)  
 fCL = 7.16MHz (CXL1505M)

Item	Symbol	Test Point	SW position				Bias condition	Conditions	Min.	Typ.	Max.	Unit
			SW1	SW2	SW3	SW4 to 7						
Autobias center level	ABCN	V1	a	b	a	a	E1	1.0	2.0	4.0	V	
Autobias black level	ABBL	V2	a	b	a	a		1.2	2.2	4.2	V	
Input source level	IS	V3	a	a	a	a		0.3	0.6	3.0	V	
CDS source level	CDS	V4	a	a	a	a		1.2	2.3	3.5	V	
Output circuit bias level	VGG	V5	a	a	a	a		0.3	0.8	3.0	V	
Supply*1 current	IDD	A1	b	a	a	a	V1		—	20	35	mA
									—	30	40	
Insertion gain	IG	V6	b	b	a to d	a	A, Bch → V1 C, Dch → V2 - 0.2V	20 log Output amplitude (mVp-p) Input amplitude (SIN 100kHz, 100mVp-p)	-4.5	-3.5	-0.5	dB
Frequency*1 response	fc	V6	c	b	a to d	a	↓	20 log Output amplitude (SIN 1MHz, 100mVp-p) Output amplitude (SIN 100kHz, 100mVp-p)	-1.8	-0.8	—	dB
Linearity	Lin.	V6	b	b	a to d	a	↓	(Note 1)	0	5	12	%
Insertion gain difference between channels	ΔG							(Note 2)	0	5	15	%
Linearity difference between channels	ΔLAB							(Note 3)	0	1	5	%
Linearity difference between channels	ΔLCD							(Note 3)	0	1	5	%
Cross talk between channels	CRT	V6	a	b	a to d	a ← b	A, Bch → V1 C, Dch → V2 - 0.2V	(Note 4)	0	1	3	%

\*1 Standard values are different between CXL1503M and CXL1505M.

**Notes)**

## 1. Linearity testing

For A channel and B channel, set input bias  $E_1$  to  $ABCN + 0.2$  [V] first, and then set it to  $ABCN$  [V] and  $ABCN - 0.2$  [V]. Then input a sine wave of 100kHz and 100mVp-p, and compare the three output amplitudes.

For C channel and D channel, set input bias  $E_1$  to  $ABBL - 0.4$  [V] first, and then set it to  $ABBL - 0.2$  [V] and  $ABBL$  [V]. Then input a sine wave of 100kHz and 100mVp-p, and compare the three output amplitudes.

The maximum output amplitude for the respective A, B, C and D channels is taken as  $S_{out\ max}$ . and the minimum output amplitude as  $S_{out\ min}$ . The linearity of the respective channels is defined as

$$L_{in} = \frac{S_{out\ max} - S_{out\ min}}{S_{out\ max} + S_{out\ min}} \times 200 \text{ [%]}$$

## 2. Calculation of insertion gain difference

As the max. insertion gain among A, B, C and D channels' is taken as  $G_{max}$  and the min. as  $G_{min}$ ., the insertion gain difference between channels becomes:

$$\Delta G = ABS \left( 1 - 10^{\left( \frac{G_{max} - G_{min}}{20} \right)} \right) \times 100 \text{ [%]}$$

## 3. Calculation of linearity difference

Define A channel linearity as  $L_A$ , and B channel linearity as  $L_B$ . We obtain the difference  $\Delta L_{AB}$  as follows.

$$\Delta L_{AB} = | L_A - L_B | \text{ [%]}$$

Similarly we obtain the linearity difference  $\Delta L_{CD}$  of C channel and D channel as follows.

$$\Delta L_{CD} = | L_C - L_D | \text{ [%]}$$

## 4. Crosstalk calculation

We take CRTa as: A channel crosstalk value only during B channel input

CRTb as: B channel crosstalk value only during A channel input

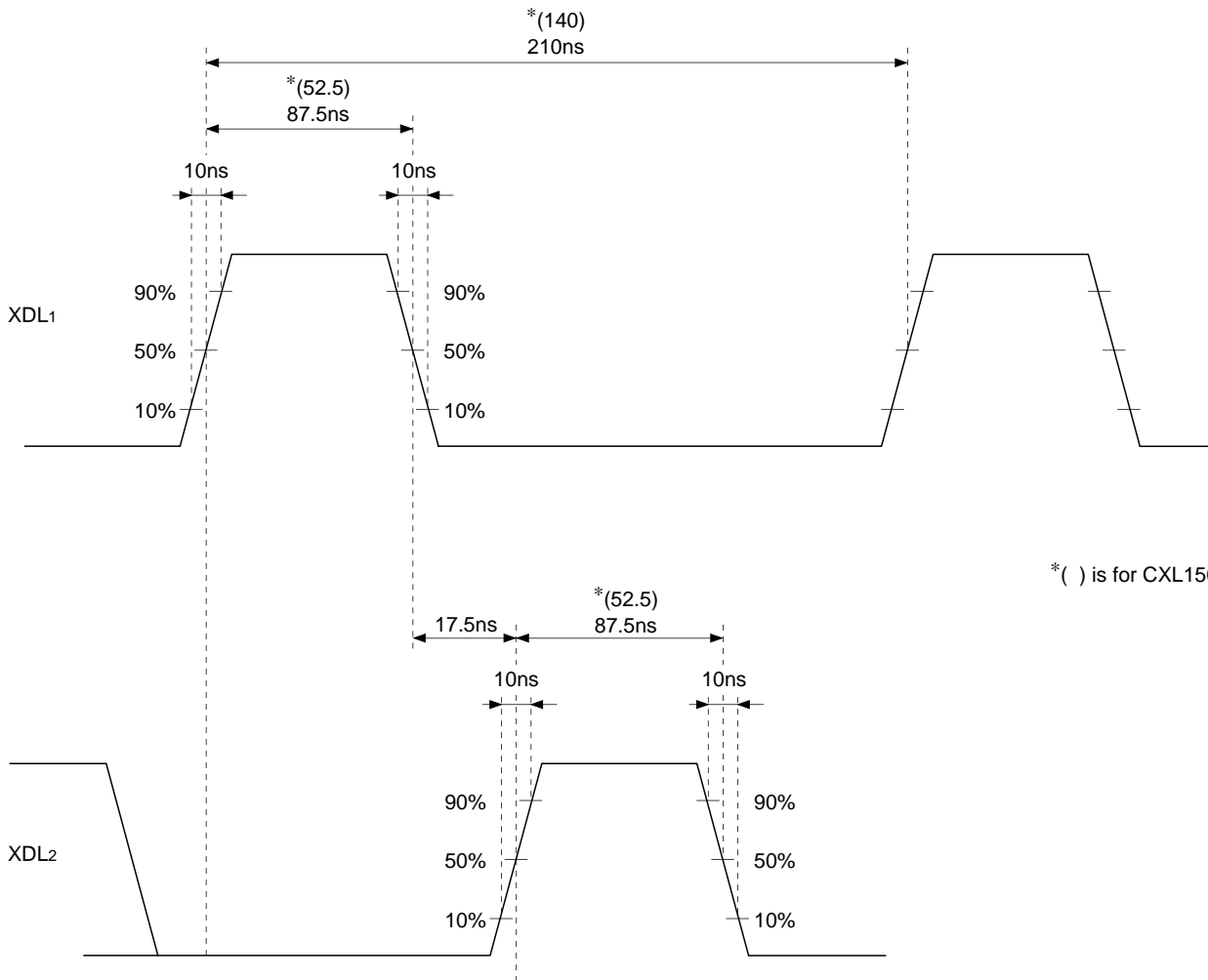
CRTc as: C channel crosstalk value only during D channel input

CRTd as: D channel crosstalk value only during C channel input

The crosstalk value of respective channels becomes:

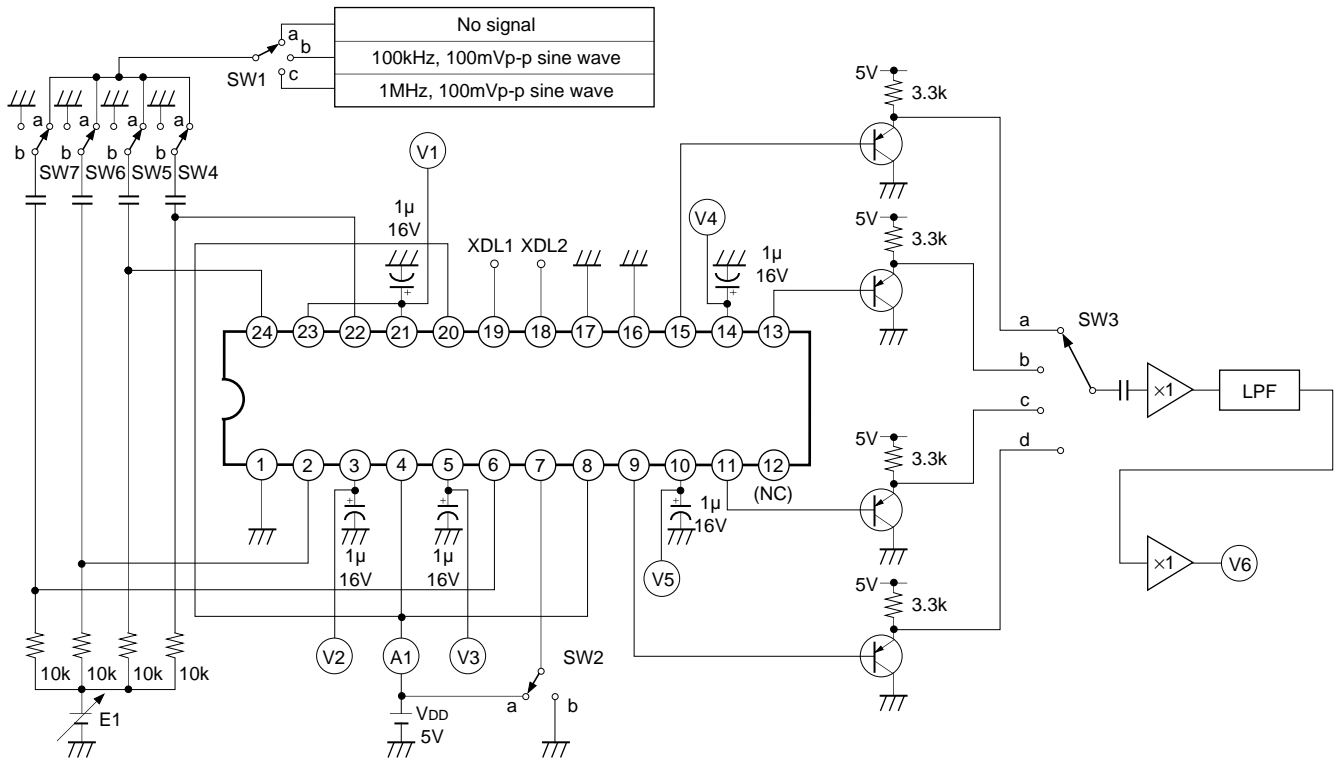
$$CRTa\ to\ d = \frac{\text{Crosstalk component}}{\text{Each channel output value}} \times 100 \text{ [%]}$$

Clock Waveform Timing

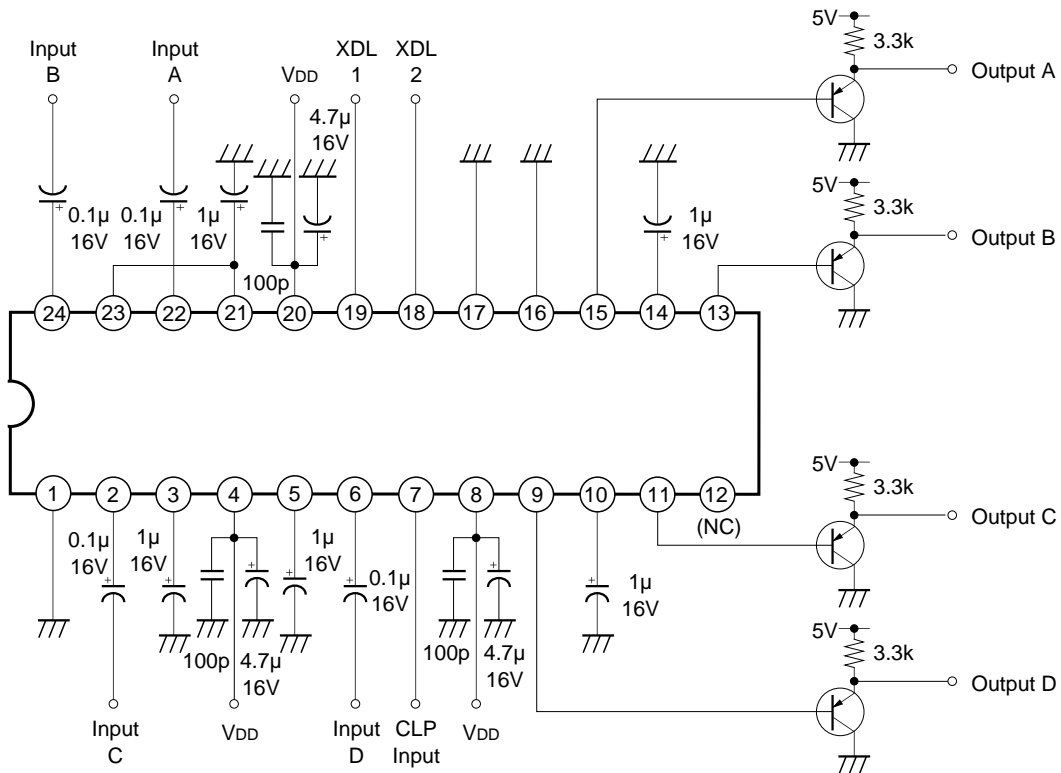


\*( ) is for CXL1505M.

Electrical Characteristics Test Circuit

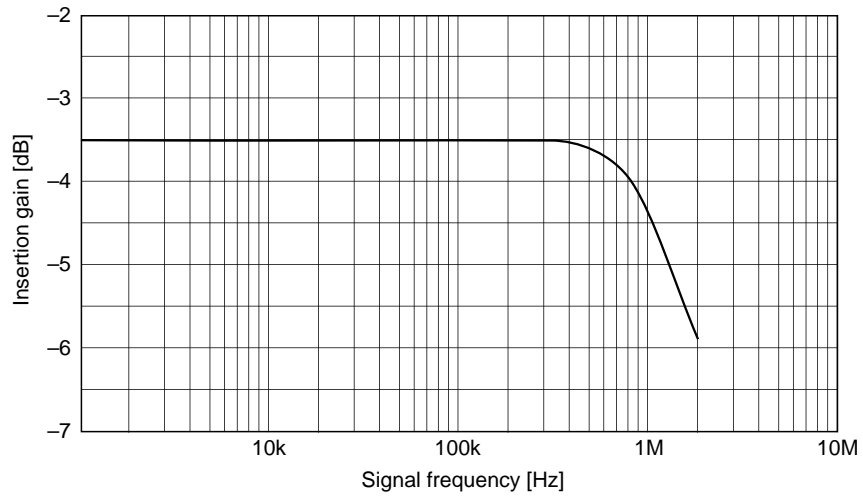


Application Circuit

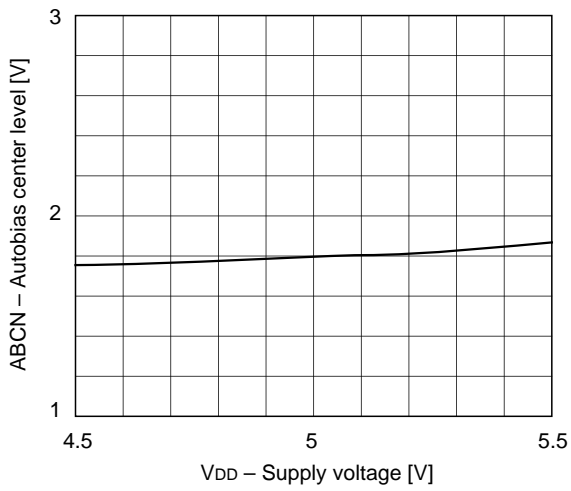


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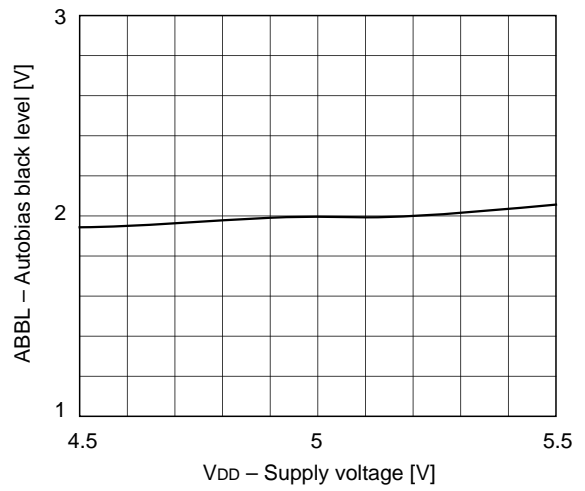
Frequency response



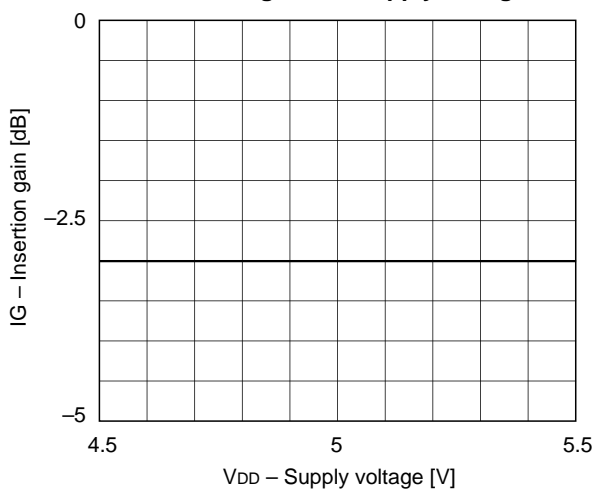
Autobias center level vs. Supply voltage



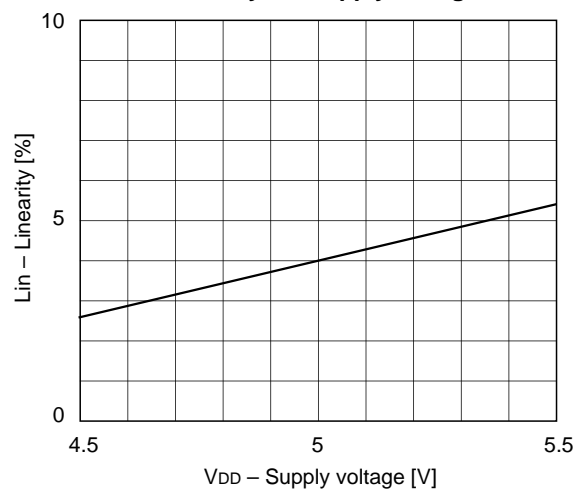
Autobias black level vs. Supply voltage

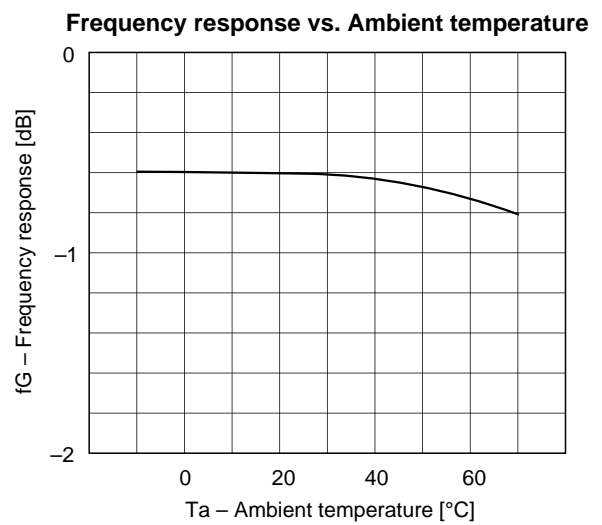
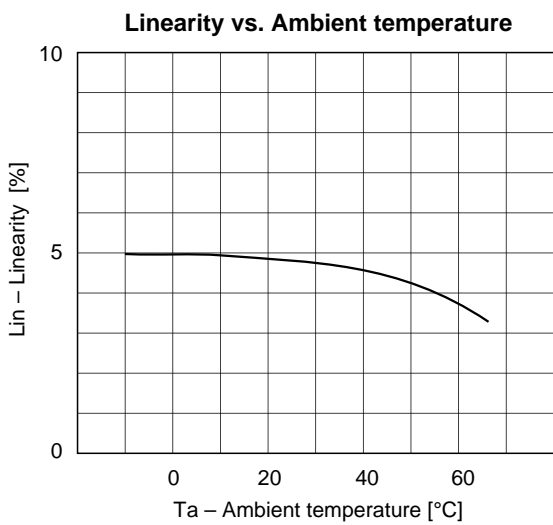
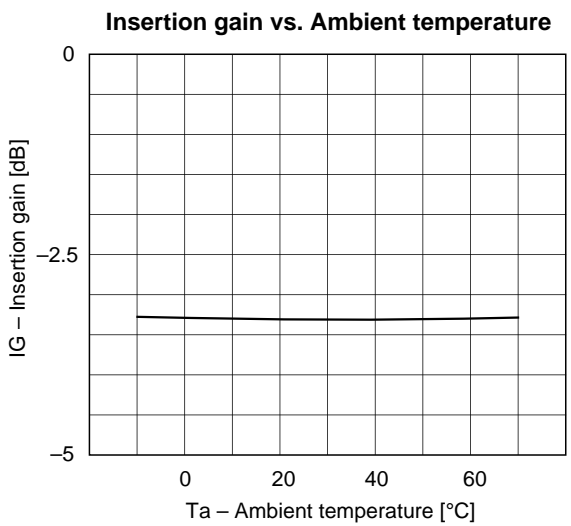
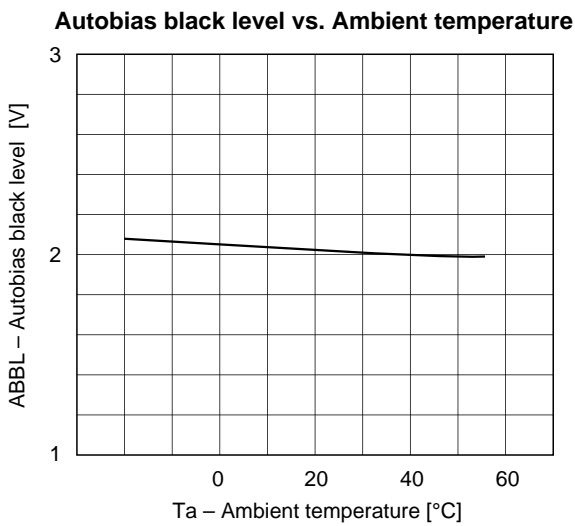
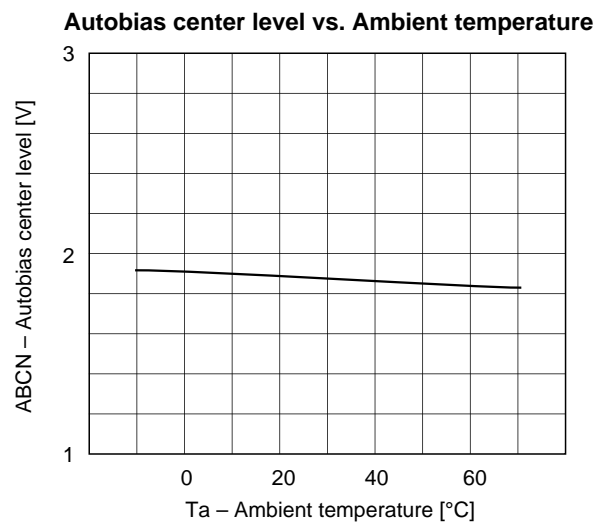
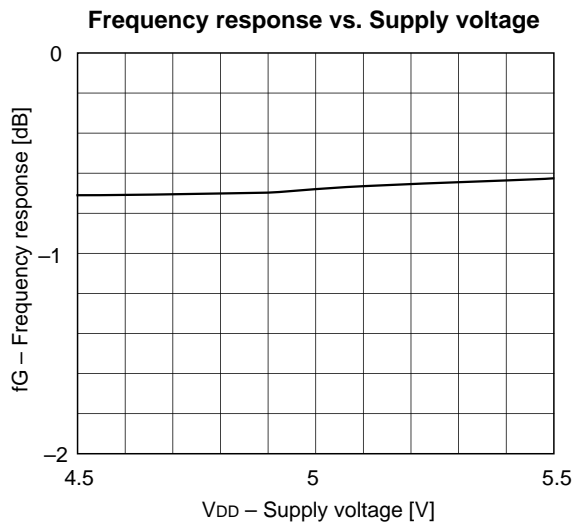


Insertion gain vs. Supply voltage



Linearity vs. Supply voltage

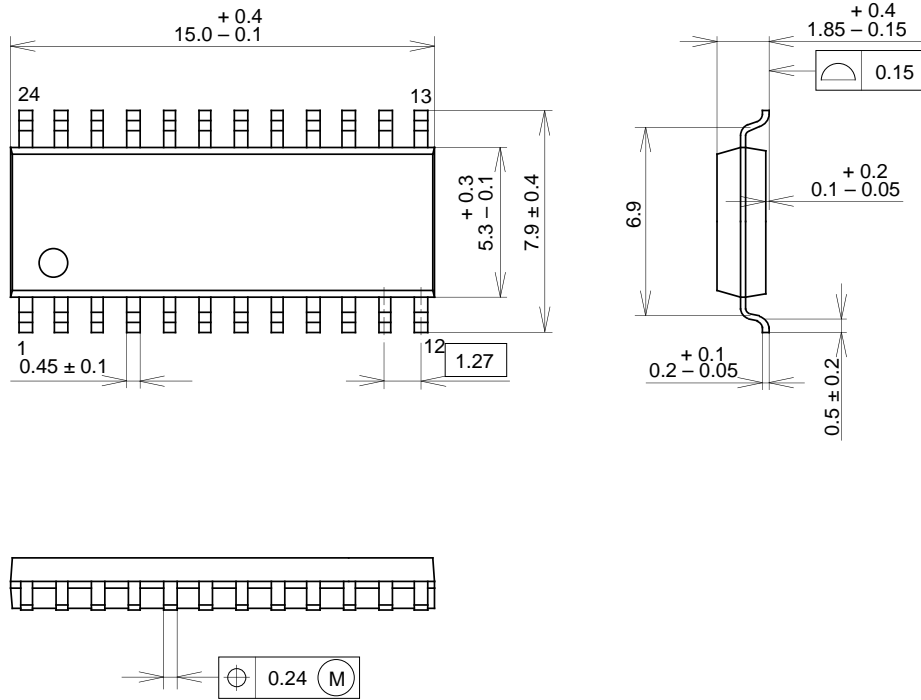






Package Outline Unit: mm

24PIN SOP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	SOP-24P-L01
EIAJ CODE	SOP024-P-0300
JEDEC CODE	_____

MOLDING COMPOUND	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.3g