5-channel BTL driver for CD players
BA6796FP

The BA6796FP, an IC designed for CD and MD players, has a 5-channel BTL power driver and a standard operational amplifier. The spindle and tray driver share a single output buffer, and are specified with a control pin. In addition, the internal level shift circuit reduces the number of attached components.

●Applications
CD players, CD-ROM drives, MD players and other optical disc devices

●Features
1) 5-channel BTL driver in a 28-pin HSOP package, allowing for application miniaturization.
2) The five drivers are turned on and off according to control pin logic combinations.
3) The tray driver operates even when the servo power supply drops.
4) Internal thermal shutdown circuit.
5) Gain is adjustable with an attached resistor.
6) Internal standard operational amplifier.

●Absolute maximum ratings (Ta = 25°C)

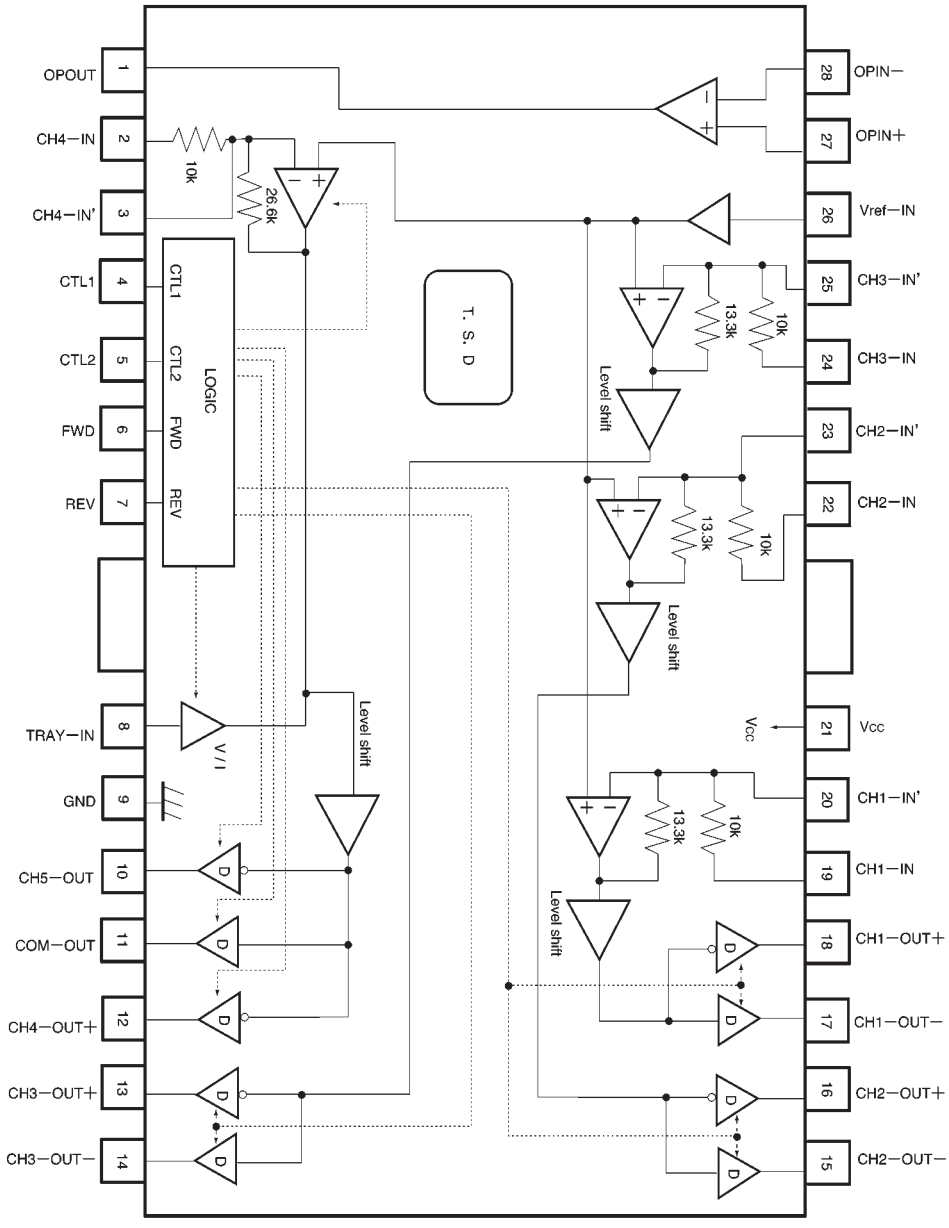
Parameter	Symbol	Limits	Unit
Power supply voltage	V_{CC}	18	V
Power dissipation	Pd	1.7*	W
Operating temperature	Topr	−35～+85	℃
Storage temperature	Tstg	−55～+150	℃

* When mounted on a 50 × 50 × 1 mm paper phenol board
Reduced by 13.6 mW for each increase in Ta of 1℃ over 25℃.

●Recommended operating conditions (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V_{CC}	4.8	—	12	V

●Block diagram

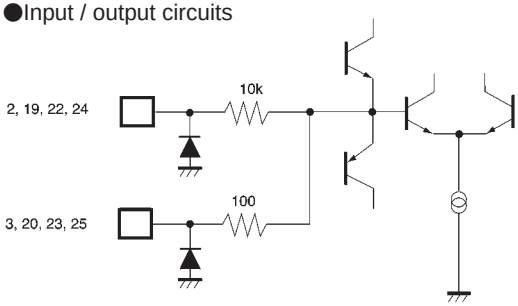


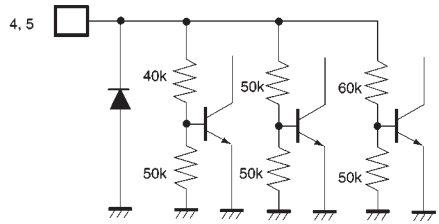
●Pin descriptions

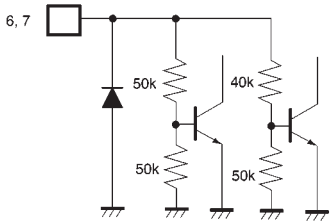
Pin No.	Pin name	Function
1	OPOUT	Operational amplifier
2	CH4−IN	Channel 4 input
3	CH4−IN'	Channel 4 gain adjustment input
4	CTL1	Control 1 input
5	CTL2	Control 2 input
6	FWD	Tray forward input
7	REV	Tray reverse input
8	TRAY−IN	Tray input
9	GND	Substrate ground
10	CH5−OUT−	Tray negative output
11	COM−OUT	Tray positive output/channel 4 negative output
12	CH4−OUT+	Channel 4 positive output
13	CH3−OUT+	Channel 3 positive output
14	CH3−OUT−	Channel 3 negative output
15	CH2−OUT−	Channel 2 negative output
16	CH2−OUT+	Channel 2 positive output
17	CH1−OUT−	Channel 1 negative output
18	CH1−OUT+	Channel 1 positive output
19	CH1−IN	Channel 1 input
20	CH1−IN'	Channel 1 gain adjustment input
21	Vcc	Vcc
22	CH2−IN	Channel 2 input
23	CH2−IN'	Channel 2 gain adjustment input
24	CH3−IN	Channel 3 input
25	CH3−IN'	Channel 3 gain adjustment input
26	VREF−IN	Bias amplifier input
27	OPIN+	Operational amplifier non-inverted input
28	OPIN−	Operational amplifier inverted input

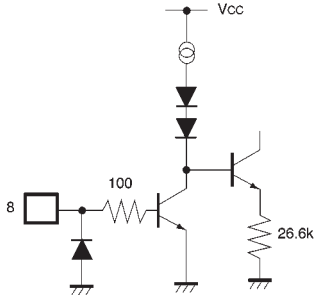
* Positive and negative output of the driver is relative to the polarity of the input pins.
(For example, pin 18 outputs the high level when the high level is input to pin 19.)

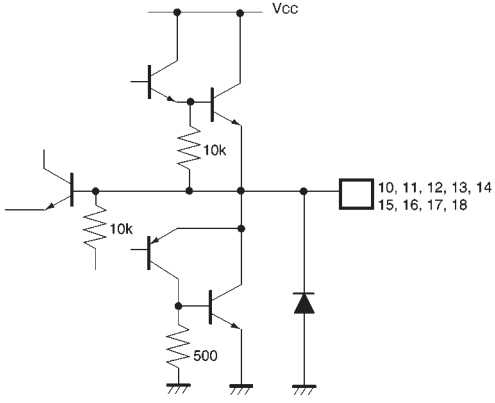
●Input / output circuits

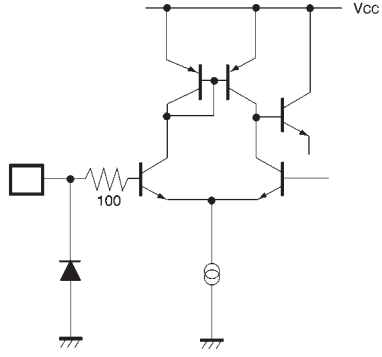


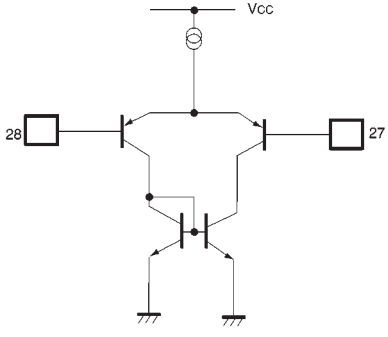












●Electrical characteristics (unless otherwise noted, Ta = 25°C, V_{CC} = 8V, f = 1kHz, R_L = 8Ω)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Quiescent current dissipation	I_{CC}	8.5	11.5	14.5	mA	No load
Output offset voltage 1	V_{OO}	−40	—	40	mV	Channel 1～Channel 3
Output offset voltage 2	V_{OO}	−100	—	100	mV	Channel 4
Max. output pin voltage 1	V_{OHD1}	3.7	4.3	—	V	V_{IN}=V_{CC}
Max. output pin voltage 2	V_{OHD2}	—	−4.3	−3.7	V	V_{IN}=GND
Closed loop voltage gain 1	G_{VC1}	6.5	8.0	9.5	dB	V_{IN}=0.1V_{rms}, 1kHz (excluding channel 4)
Closed loop voltage gain 2	G_{VC2}	11.5	14.0	16.5	dB	V_{IN}=0.1V_{rms}, 1kHz (CH4)
Ripple rejection rate	RR	—	60	—	dB	V_{IN}=0.1V_{rms}, 100Hz
Slew rate	SR	—	2.0	—	V/μs	100 Hz square wave, 3 V_{P-P} output
〈Tray driver〉						
Output voltage F	V_{OF}	2.5	3.0	3.5	V	Pin 8 voltage=3 V
Output voltage R	V_{OR}	−3.5	−3.0	−2.5	V	Pin 8 voltage=3 V
Output voltage range F	V_{OMF}	3.7	4.3	—	V	Pin 8 voltage=5 V
Output voltage range R	V_{OMR}	—	−4.3	−3.7	V	Pin 8 voltage=5 V
Load regulation F	$\triangle V_{FI}$	—	250	500	mV	I_L=100～400 mA, pin 8 voltage=2.5 V
Load regulation R	$\triangle V_{RI}$	—	250	500	mV	I_L=100～400 mA, pin 8 voltage=2.5 V
Line regulation F	$\triangle V_{FL}$	—	300	600	mV	V_{CC}=5V～12V
Line regulation R	$\triangle V_{RL}$	—	300	600	mV	V_{CC}=5V～12V
Output offset voltage	V_{OOL}	−50	—	50	mV	Braked, output voltage
〈Logic: CTL1, CTL2, FWD, REV〉						
Input high level voltage	V_{IH}	2.0	—	8.0	V	Maximum value up to Vcc
Input low level voltage	V_{IL}	−0.3	—	0.5	V	
Input high level current	I_{IH}	—	—	500	μA	
Input low level current	I_{IL}	—	—	500	μA	
〈Operational amplifier〉						
Offset voltage	V_{OFOP}	−5	0	5	mV	
Input bias current	I_{BIAS}	—	—	300	nA	
Output high level voltage	V_{OHOP}	6.0	—	—	V	
Output low level voltage	V_{OLOP}	—	—	1.8	V	
Output drive current (source)	I_{OSO}	10	40	—	mA	50Ω at GND
Output drive current (sink)	I_{OSI}	10	50	—	mA	50Ω at V_{CC}
Open loop voltage gain	G_{VO}	—	78	—	dB	V_{IN}=−75dBV, 1kHz
Slew rate	SR_{OP}	—	1	—	V/μs	100 Hz square wave, 4 V_{P-P} output
Ripple rejection	RR_{OP}	—	65	—	dB	V_{IN}=0.1V_{rms}, 100Hz
Common mode rejection ratio	CMRR	—	84	—	dB	V_{IN}=0.1V_{rms}, 1kHz

◎Not designed for radiation resistance.

●Measurement circuit

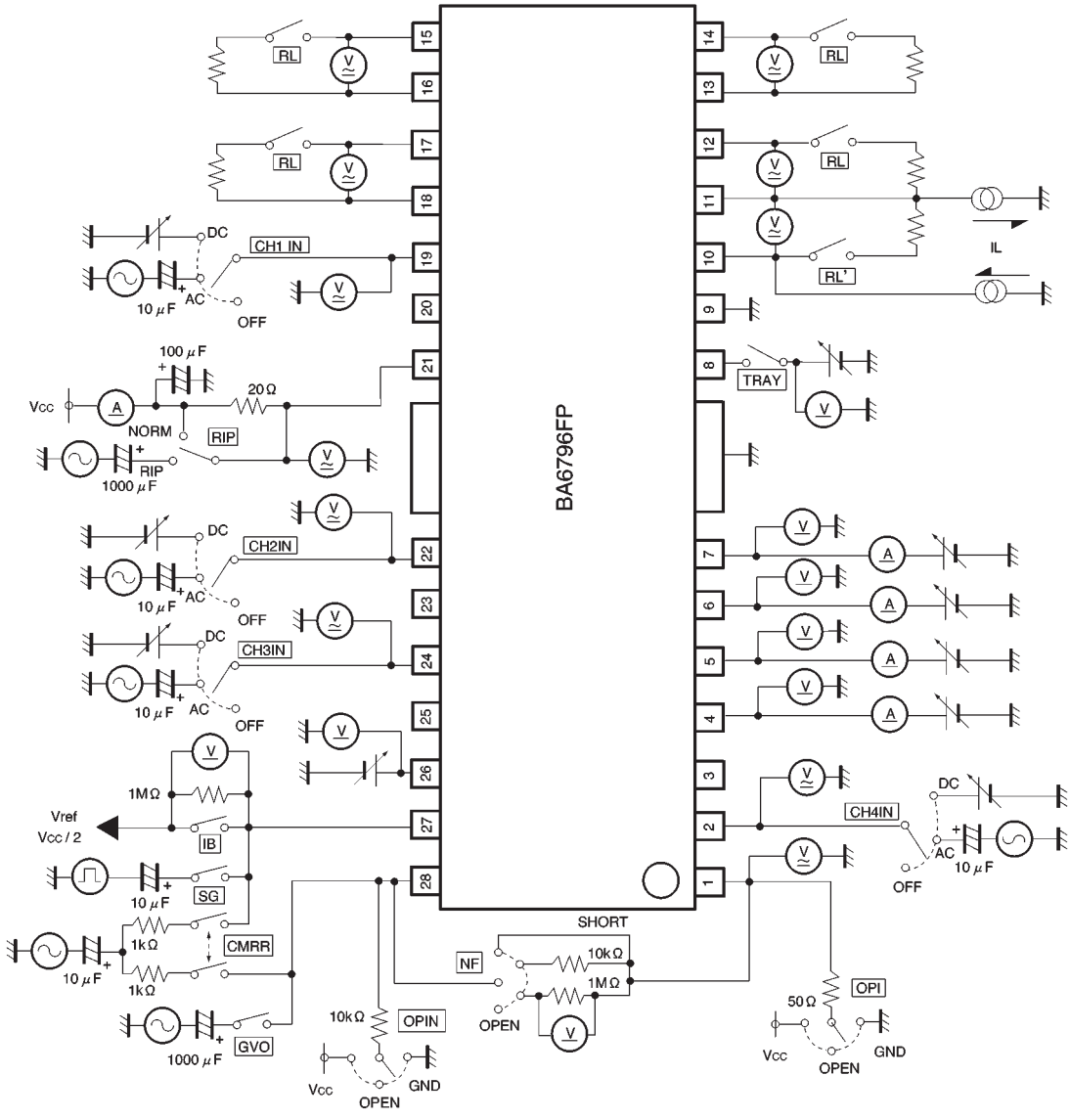


Fig.1

●Measruement circuit switch table

Parameter	Symbol	RL	RL'	CH1IN	CH2IN	CH3IN	CH4IN	TRAY	NF	IB	OPIN	OPI	GVO	RIP
Quiescent current dissipation	I_{CC}	OFF		OFF				OFF	SHORT	ON	OPEN	OPEN	OFF	NORM
Output offset voltage	V_{OO}	ON		DC (BIAS)				↓	↓	↓	↓	↓	↓	↓
Max. output pin voltage 1	V_{OHD1}	↓		DC (GND)				↓	↓	↓	↓	↓	↓	↓
Max. output pin voltage 2	V_{OHD2}	↓		DC (V_{CC})				↓	↓	↓	↓	↓	↓	↓
Closed loop voltage gain 1	G_{VC1}	↓		AC (0.1V_{rms}, 1kHz)				↓	↓	↓	↓	↓	↓	↓
Closed loop voltage gain 2	G_{VC2}	↓		↓				↓	↓	↓	↓	↓	↓	↓
Ripple rejection rate	RR	↓		DC (BIAS)				↓	↓	↓	↓	↓	↓	RIP
Slew rate	SR	↓		AC (100 Hz square wave)				↓	↓	↓	↓	↓	↓	NORM
〈Tray driver〉														
Output voltage F	V_{OF}	ON		DC (BIAS)				ON	SHORT	ON	OPEN	OPEN	OFF	NORM
Output voltage R	V_{OR}	↓		↓				↓	↓	↓	↓	↓	↓	↓
Output voltage range F	V_{OMF}	↓		↓				↓	↓	↓	↓	↓	↓	↓
Output voltage range R	V_{OMR}	↓		↓				↓	↓	↓	↓	↓	↓	↓
Load regulation F	$\triangle V_{FI}$	ON	OFF	↓				↓	↓	↓	↓	↓	↓	↓
Load regulation R	$\triangle V_{RI}$	↓	↓	↓				↓	↓	↓	↓	↓	↓	↓
Line regulation F	$\triangle V_{FL}$	ON		↓				↓	↓	↓	↓	↓	↓	↓
Line regulation R	$\triangle V_{RL}$	↓		↓				↓	↓	↓	↓	↓	↓	↓
Output offset voltage	V_{OOL}	↓		↓				↓	↓	↓	↓	↓	↓	↓
〈Logic: CTL1, CTL2, FWD, REV〉														
Input high level voltage	V_{IH}	OFF		OFF				OFF	SHORT	ON	OPEN	OPEN	OFF	NORM
Input low level voltage	V_{IL}	↓		↓				↓	↓	↓	↓	↓	↓	↓
Input high level current	I_{IH}	↓		↓				↓	↓	↓	↓	↓	↓	↓
Input low level current	I_{IL}	↓		↓				↓	↓	↓	↓	↓	↓	↓
〈Operational amplifier〉														
Offset voltage	V_{OFOP}	OFF		OFF				OFF	SHORT	ON	OPEN	OPEN	OFF	NORM
Input bias current	I_{BIAS}	↓		↓				↓	1M	OFF	↓	↓	↓	↓
Output high level voltage	V_{OHOP}	↓		↓				↓	10k	ON	GND	↓	↓	↓
Output low level voltage	V_{OLOP}	↓		↓				↓	↓	↓	V_{CC}	↓	↓	↓
Output drive current (source)	I_{OSO}	↓		↓				↓	SHORT	↓	OPEN	GND	↓	↓
Output drive current (sink)	I_{OSI}	↓		↓				↓	↓	↓	↓	V_{CC}	↓	↓
Open loop voltage gain	G_{VO}	↓		↓				↓	10k	↓	↓	OPEN	ON	↓
Slew rate	S_{ROP}	↓		↓				↓	SHORT	OFF	↓	↓	OFF	↓
Ripple rejection	R_{ROP}	↓		↓				↓	↓	ON	↓	↓	↓	RIP
Common mode rejection ratio	C_{MRR}	↓		↓				↓	1M	OFF	↓	↓	↓	NORM

∗1 Switch SG is on only when measuring the operational amplifier's SRop.

∗2 Switch CMRR is on only when measuring the operational amplifier's CMRR.

●Function description

CTL and CTL2

CTL1	CTL2	CH1	CH2	CH3	CH4	CH5
L	L	OFF				ON
L	H					
H	L	ON				OFF
H	H	OFF		ON	OFF	ON

● High-impedance output when off.

F and R (channel 5 control enabled only when channel 5 is on)

F	R	Output mode
L	L	High impedance
L	H	Reverse
H	L	Forward
H	H	Brake

●Application example

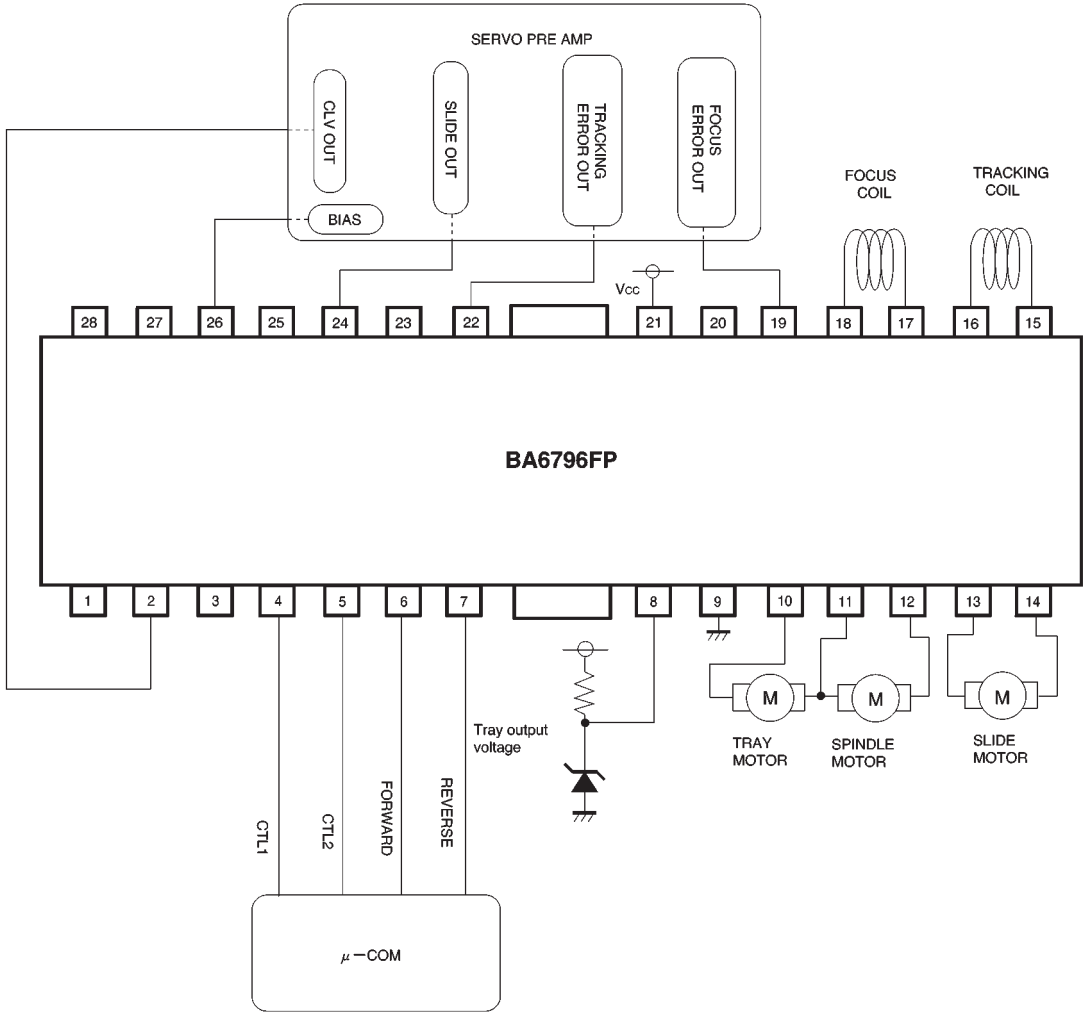


Fig. 2

●Operation notes

(1) Setting the tray motor driver voltage (forward mode)

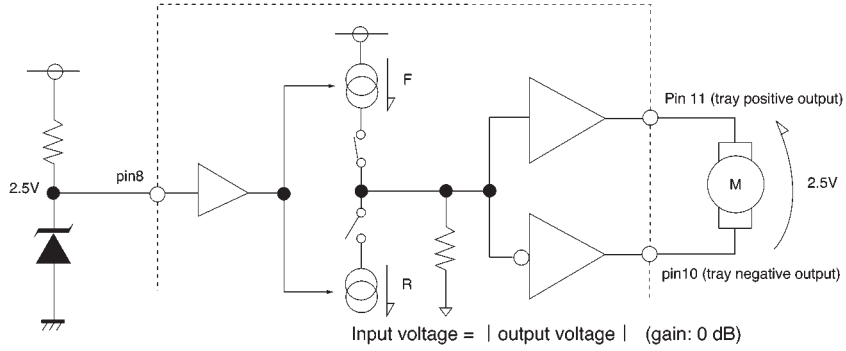


Fig. 3

Note: The tray driver output voltage will not exceed the power supply's maximum output voltage, even if set above this maximum voltage (refer to the following page). The example above applies only when setting below the maximum output voltage. Maximum output voltage for the power supply can be output by pulling up the tray input pin (pin 8), or by connecting it to Vcc.

(2) Mute functions

Mute function	Muted channels
Thermal shutdown	All channels
Muting during supply voltage drop	All channels
Muting during bias voltage drop	CH1-CH4

≪Thermal shutdown≫

The output current is muted when the chip temperature exceeds 175°C (typically).

≪Supply voltage drop muting≫

The internal circuits turn off when the supply voltage drops below 4.3V (typically), and turn on again when it rises above 4.5V (typically).

≪Bias drop muting≫

Muting also occurs when the bias pin voltage (26 pin) is lowered below 1.4V (typically). Be sure the voltage stays between 1.6V and 6.5V during normal operation.

(3) Muting occurs during thermal shutdown and when the supply voltage or bias pin voltage drops. In each case, only the driver is muted. The output pin voltage during muting is the internal bias voltage, roughly $V_{CC}-V_F/2$.

(4) Attach a 0.1µF bypass capacitor to the power supply, at the base of the IC.

(5) Connect the radiating fin to an external ground.

●Electrical characteristic curves

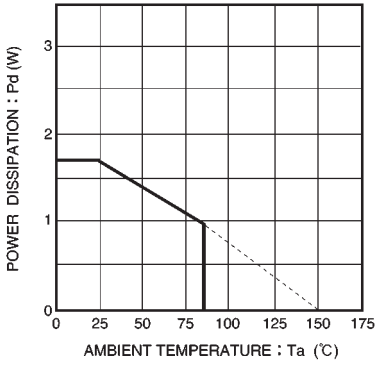


Fig. 4 Thermal derating curve

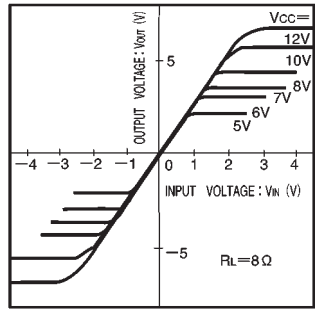


Fig. 5 CH1-CH-3 Driver I / O characteristics (when variable supply voltage changes)

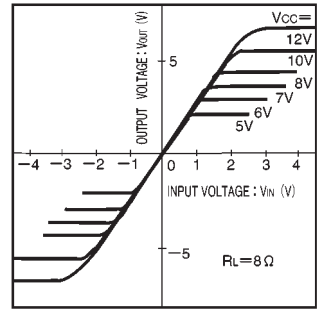


Fig. 6 CH4 Driver I / O characteristics (when variable supply voltage changes)

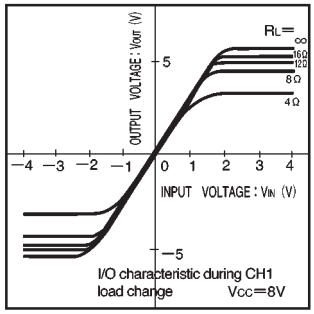


Fig. 7 CH1-CH3 Driver I / O characteristics (when load changes)

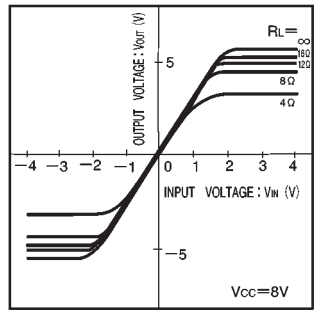


Fig. 8 CH4 Driver I / O characteristics (when load changes)

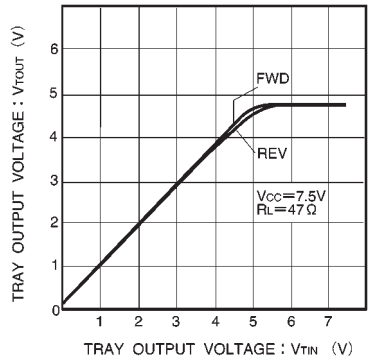


Fig. 9 Tray driver output characteristics

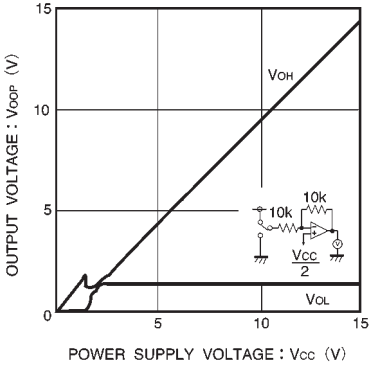


Fig. 10 Power supply voltage vs. HIGH output / LOW output voltage

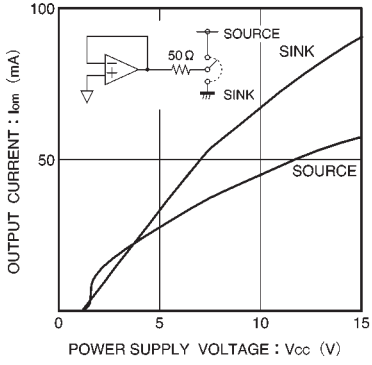


Fig. 11 Power supply voltage vs.operational amplifier output operating current

●External dimensions (Units: mm)